

A Design of Application Based Wireless Sensor Node

Sham P Nayse

PHD scholar, Dept Computer Science,
 SGBA University Amravati, India.
 shamnayse@gmail.com

Mohammad Atique

Associate Prof., Dept Computer Science,
 SGBA University Amravati, India.
 mohd.atique@gmail.com

Abstract— Proposed wireless sensor node is a highly flexible and programmable system on chip (PSoC) architecture along with integrated RF radio chip, which can be adapted to any IEEE 802.15.4 standard based protocol, working at the band of 2.4GHz. This can be accompanied by the RF antenna matched with the interface circuit for various kinds of sensors and peripherals to form a wireless sensor node. This can be very well used to form a wireless sensor network in different domains. This proposed methodology can be used for specific application for improving the WSN stability and performance. This article will mainly present the design of wireless sensor nodes based on PSoC and CyFi radio chip, including the application specific antenna and hardware design for the system on chip for the sensor node and the simple introduction of the application domain. The proposed nodes are used with a special antenna and application based protocol for communication. This design has a better power handling and performing capacity. Further, we have implemented this for the wireless sensor node as well.

Keywords—PSoC, CyFi, wireless sensor network; cost effective wireless sensor nodes;

I. INTRODUCTION

The System on chip SoC is the arrival of the new technological revolution; the world enters the information and VLSI age. To make use of the information, the first thing that we must do is to obtain accurate and reliable data. We can use sensors to obtain information in the natural parameters with low power and low overhead fields in data communication.

WSN has already penetrated into numerous areas such as industrial production, space development, ocean exploration, environmental protection, resource survey, medical diagnostics, biotechnology, and even conservation, etc. It is no exaggeration to say that, from the deep ocean to the vast space, along with a variety of complex engineering systems and every modern project, is inseparable from a variety of sensors.

The Wireless Sensor Network is composed of a set of sensor nodes. The sensor nodes form the communication network in the of multi-hop and self organization fashion[1]. Using sensor nodes and its network, the information of the monitored objects are distributed to the target area, which can then be collected. This collected information will pass to the upper layer of wireless communication stack in an abstracted way. Therefore, it is very important to design a kind of efficient and practical wireless sensor node [3].

II. THE OVERALL STRUCTURE OF WIRELESS SENSOR NETWORK SYSTEM

The wireless sensor network system architecture is as shown in figure 1. It has three parts; (1) sensor nodes; (2) the sink node/ WSN gateway; (3) monitoring center [3]. Sensor nodes have the capabilities such as data acquisition, signal processing and wireless communication. It is both: the initiator and the transmitter of the information frame. The Self deviser Network which is self-organized and has multi-hop routes sends the collected monitoring data to the WSN gateway. WSN gateway, also known as convergent node, transmits the data collected by the sensor nodes to the monitoring center through the serial communication; The terminal monitoring center mainly carries out tasks such as managing and questing the data from the network, sending the networking request, asking the specified nodes to sample data ,etc. But in the task, the function and the terminal monitoring center is divided into two parts: data acquisition and data management. Figure 1 shows the over all picture of wireless sensor network. These have no of sensors nodes.

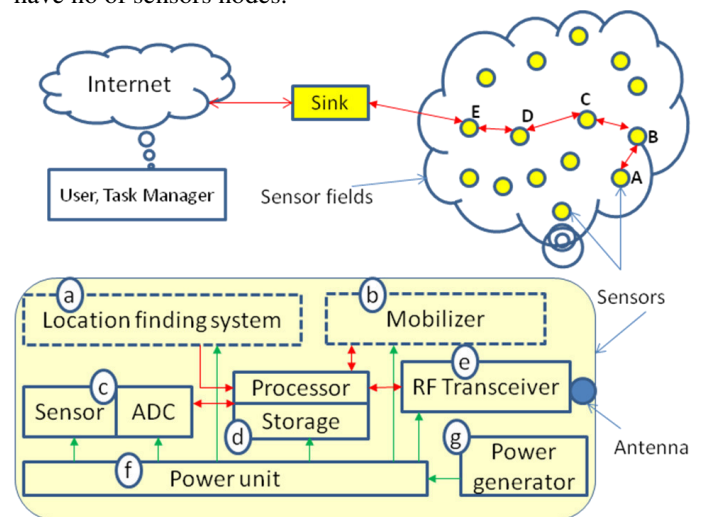


Figure 1: Architecture of Wireless Sensor Network

III. HARDWARE DESIGN

There Wireless sensor nodes (part a to g of Figure 1) are the key part of sensor network. The node is generally made up of data collecting unit (c), data processing (d) and transmitting unit (e). These are three essential parts which are shown in

figure 1. The next parts are location finding system (a) and mobilizers (b), which are required for the moving object application. In fact there are two more parts which too play a very important role in wireless sensor node. These are: antenna which is a part of the transmitting unit, and battery (g) which supplies power to all. Data collecting unit is responsible for collecting information within the monitoring area and completing the data conversion from the analog value to its digital value. The wireless sensor nodes achieve the acquisition of different physical quantities by being equipped with different sensor modules. Data processing and transmitting unit consists of two modules: data processing and data transmitting.

The central processing unit (CPU) is responsible for controlling and handling the routing protocol, simultaneous localization and power management of the entire sensor node; The data transmitting module is responsible for conducting wireless communication with other nodes, exchanging controlled messages, sending and receiving the collected data, and so on and so forth. The data transmitting unit mainly consists of corresponding communication protocols (mainly MAC or physical level protocol) and low-power; short range wireless communication module and antenna [4]

Data processing and protocol management units makes use of the program and data memory of PSoC device which integrates with the CPU core with a choice of M8C, 8051 or ARM as shown in Table 1. Data acquisition components like PA (programmable gain amplifier), ADC, multiplexer, programs routine and protocol stack (Tiny OS) can transmit data wirelessly, as further described in the next section. Data processing and transmitting unit is the core of the application specific wireless sensor node, which is responsible for collecting the parameters of various required physical quantities or signals. It requires sampling rate and certain amount of data. The choice of processor is crucial while designing the node.

PSoC family & CyFi is a true and flexible, programmable and reconfigurable system on radio chip (SoC) of CMOS solution [9]. This solution can improve performance and meet the application goal with IEEE 802.15.4 based 2.4GHz ISM band and can meet the request of low cost and low power. It combines with a high performance 2.4GHz DSSS (Direct Sequence Spread Spectrum) RF transceiver CyFi and a compact and efficient PSoC device. The design of the PSoC combines the 8 to 64 Kbyte RAM and powerful library of user modules [10].

Table 1: PSoC Family and features

PSoC 1	PSoC 3	PSoC 4	PSoC 5
Performance optimized 8-bit M8U	Performance optimized single cycle 8-bit 8051 core	High-performance 32-bit ARM Cortex-M0	High-performance 32-bit ARM Cortex-M3
Up to 24 MHz, 4 MIPS Flash 4 KB to 32 KB SRAM 256 bytes -2 KB Operation 1.7 V- 5.25 V	Up to 67 MHz, 33 MIPS Flash 8 KB to 64 KB SRAM 3 KB to 8 KB Operation 0.5 V to 5.5 V	Up to 48 MHz, MIPS Flash 16 KB to 32 KB SRAM 4 KB Operation 1.71 V to 5.5 V	Up to 67 MHz, 84 MIPS Flash 32 KB to 256 KB SRAM 16 KB to 64 KB Operation 2.7 V to 5.5 V
1 Delta-Sigma ADC (6 to 14-bit) 131 ksps @ 8-bit Voltage Precision $\pm 1.53\%$ Up to two DACs (6 to 8-bit)	1 Delta-Sigma ADC (8 to 20-bit) 192 ksps @ 12-bit Voltage Precision $\pm 0.1\%$ Up to four DACs (8-bit)	1 SAR ADC (12-bit) 1 Msps @ 12-bit Up to 2 DACs (8-bit)	1 Delta-Sigma ADC (8 to 20-bit); 2 SAR ADCs (12-bit) 192 ksps @ 12-bit; 1 Msps @ 12-bit Voltage Precision $\pm 1.0\%$ Up to four DACs (8-bit)
Active: 2 mA, Sleep: 3 μ A FS USB 2.0, I ² C, SPI, UART	Active: 1.2 mA, Sleep: 1 μ A, Hibernate: 200 nA FS USB 2.0, I ² C, SPI, UART, CAN, LIN, I ² S	Active: 1.6 mA, Sleep: 1.3 μ A, Hibernate: 150 nA I ² C, SPI, UART	Active: 2 mA, Sleep: 2 μ A, Hibernate: 300 nA FS USB 2.0, I ² C, SPI, UART, LIN, I ² S
Requires ICE Cube and FlexPods	On-chip JTAG, Debug and Trace; SWD, SWV	On-chip JTAG, Debug and Trace; SWD, SWV	On-chip JTAG, Debug and Trace; SWD, SWV
Up to 64 I/O	Up to 72 I/O	Up to 36 I/O	Up to 72 I/O

There are three different architectures for the selection of CPU core. These depend on different members of PSoC

families like PSoC-1 with M8C core, PSoC-3 8051 core, PSoC-4 low power Cortex-M0, PSoC-5 Cortex-M3. Each of

the members has option of flash memory space such as 32,64 and 128 k Byte and the digital and analog block to optimize the combination of complexity and cost. The device size ranges from 7×7 mm 48-pin package. It uses the 0.18 & micro CMOS standard technology with embedded flash memory. This can be integrated with different choices of user module which fix either in digital or analog array. The proposed node extends the use of the previous architecture of PSoC-1 to higher families, either to PSoC3 or PSoC-4 chip for improving the processing capability of the sensor node. The separate part CyFi can be the RF front end for any device of the PSoC, memory and microcontroller in a single chip. It uses an 8-bit to 32 bit architecture on selection of PSoC family, with 128-64 KB programmable flash memory and 8-64 KB RAM. It further includes analog-digital arrays for ADC, DAC, Filters, analog amplifiers, timers, PWM, counter, comparator, watchdog Timer, different clock, grounding flexibility Power section, power monitoring, with sleep mode timer, power On Reset, brown out detection, and up to 72 programmable I/O pins. Choice of user module can be added in the hibernate mode for the better performance of power aware sensor node design [2], the detail classification of which is shown in table 1.

This is the latest PSoC-4 device chip using recent and latest CMOS process technology. The current consumption in the receiving and transmitting mode, is lower than 1.2 mA or 25 mA . Sleep mode and the characteristics that can use very short time to complete the mode conversion is especially suitable for the applications which require long battery life.

The main features of the CyFi chip are as follows:

CyFi is a 2.4-GHz direct sequence spread spectrum (DSSS) & GFSK radio transceiver. It operates in the unlicensed worldwide industrial, scientific, and medical (ISM) band (2.400 GHz to 2.483 GHz). Its operating current is 21 mA (transmit at -5 dBm) and sleep current is less than 1 μ A. The transmit power is up to +4 dBm and receiver's sensitivity is up to -97 dBm. CyFi can operate in DSSS modulation techniques with data rates up to 250 kbps. With the Gaussian frequency-shift keying (GFSK) modulation it can go up to 1 Mbps data rate. It requires less external component count that is only crystal and antenna matching circuit for impedance matching [10]. CyFi even supports new advanced features like auto transaction sequencer (ATS) - no MCU intervention, framing, length, CRC16, auto acknowledge (ACK), power management unit (PMU) for MCU, fast startup and fast channel changes for hopping. It has separate 16 byte transmitter, and receiver FIFO buffers. It has a dynamic data rate reception, which receives signal strength indication (RSSI). CyFi can communicate with PSoC devices with serial peripheral interface (SPI). It can be controlled while in sleep mode also. It has a microcontroller interface of 4-MHz SPI. It has in built battery voltage monitoring circuitry which can support even coin-cell operated applications because of its operating voltage which ranges from 1.8 V to 3.6 V with temperatures from 0 $^{\circ}$ C to 70 $^{\circ}$ C. It is available in very small space saving package 40-pin QFN 6×6 mm. The actual node of this configuration is shown in figure 2. It is exactly the size of Nokia rechargeable battery and can fit at the rear side of the node. It can be used as a standard node in the low cost solution for laboratory or field.

This node has a high degree integration however its work architecture is simple (as it is shown in figure 1). If the PSoC device and CyFi chip is coupled with a small number of electronic components and sensor (temperature), it can become a good versatile node as shown in Figure 2 . It will be able to send and receive wireless data. In the figure, the CiFy module leads to two sets of interfaces: one with SPI to PSoC device and the other to antenna. The antenna in the figure is $\lambda / 4$ dipole antenna and patch type application specific will be the better option [4], It also can increase communication distance by the way of increasing common used antennas. The $\lambda / 4$ dipole patch antenna length can be calculated as:

$$L = 14250 / f$$

The unit of f is MHz, the length unit is cm, therefore the length of 2450MHz antenna is 2.9 cm. The length of the antenna is 2.9cm, as shown in figure 2. If the antenna is shorter, it will affect the communication distance of RF modules. The WSN gateway conducts level translation by the other wire network, this option is also available in PSoC chip, depending on the serial ports and the computer program used to communicate.

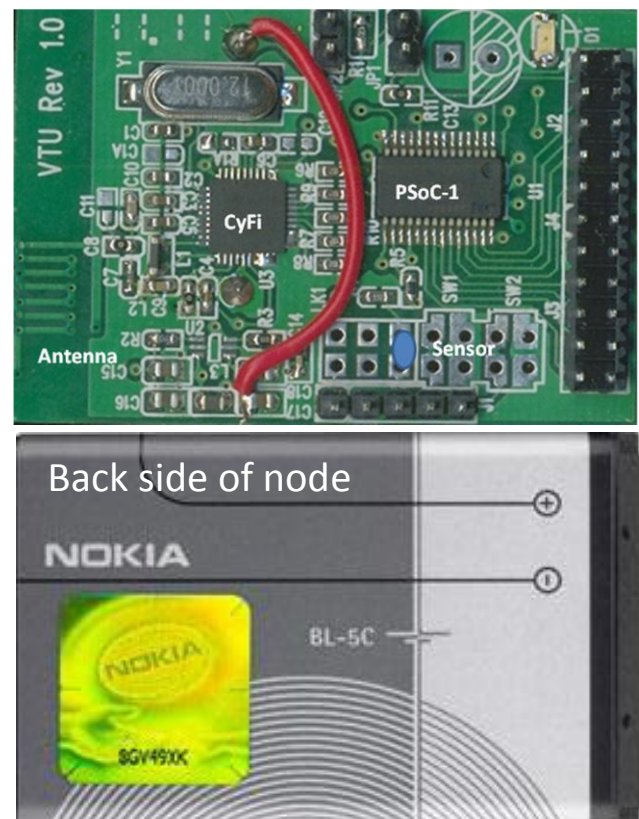


Figure 2: Proposed node

In this way the CyFi module can connect with a number of sensors through PSoC device, which can be selected as per the application requirement like light sensors, temperature sensors, etc. A typical design of the circuit is shown in Figure 4. The program and the user module selection for the

application specific wireless sensor node are flexible. It should be noted that all the required components are user selectable and controlled in programs. Even the key parameter like gain of opamp, band pass filter frequency channel freq, channel bandwidth, etc, can be changed dynamically using application specific protocol for communication. The CyFi can support the change in the channel frequency while communication with very narrow band with about 1 MHz. Thus, in the entire ISM band, user can get the felicity hoop channels of an interval of 1 MHz. In other way CyFi can support the 98 channels for communication with 1 MHz bandwidth of each [10].

IV. SOFTWARE DESIGN

Figure 3 shows the software of these types of sensor nodes. These have are four layers. 1. Tiny OS, 2. Application Specific Communication Protocol, 3. Control logic in C for switching the various user modules in PSoC device. 4. Build and configure code as per user routing and selection. Its part one is the compiler environment used by the program, i.e the TinyOS. TinyOS is an open source OS developed by UC Berkeley, which is specifically designed for embedded wireless sensor network. This operating system, based on the architecture of component makes rapid update possible, which in turn reduces the code length [1,3,6]. TinyOS components include network protocols, distributed servers, sensor-driven and data identification tools. It has a good power management due to the event-driven execution model. The model also allows flexibility for scheduling, and can even be applied to several hardware independant platforms.

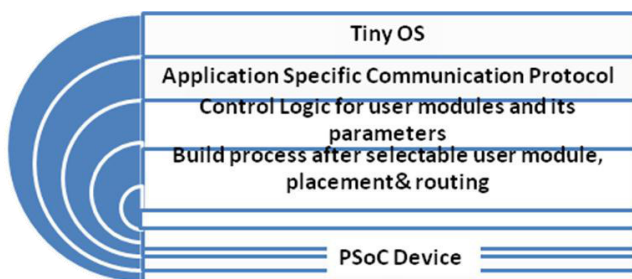


Figure 3: Layers of software development process

The layered architecture of TinyOS's component-based makes reduction of application possible to be achieved [8]. It only needs to compile the useful components for an application. A specific application usually has a top-level configuration file, completes the connections between component interfaces, and then assembles the component into a specific application. Components contain configuration and module. The achievement of configuration describes the connection of interfaces, commands or events between different components specifically. Top-level is an accessory of configuration file. The achievement of module describes commands and event functions specifically. Interface is a two-way channel between the components. Through stating a set of commands and event function, it does the interfacing for the

different functions and the event notification. Interface provider is responsible for improving the interface commands. Interface user is responsible for using interface events. An interface can be provided and called by multiple components.

The part 2 and 3 has to be done in the C programming and it varies as per the application requirement. This software portion of the sensor network nodes is mainly responsible for collecting the physical sensor data and controlling CyFi transceiver modules through instructions received from Tiny OS. This can be done with the help of PSoC creator or designer. The part 4 of the software is the building process in cypress designer or creator, used for generating build code after the selection and placement of user modules in programmable array block of PSoC. As per the requirement of the application, the user can select appropriate user module and can place it at a proper place of diital and analog array. He can then rout the connection between user modules and I/O pins. Even after the code is built, the user programme (C code) can keep the changes in the key parameters dynamically and can improve the performance of the node and network in power prospective, accuracy and so on [2].

The basic idea of the system software programming is that the PSoC devices is initialized, which sets the mux input and gain of programmable amplifier. Sampling clock of the ADC, sets the timer. The then timer does AD conversion on the sensor at regular intervals through the selected ADC input channel, and fills the data into data packets. It then sends the data packets through the CyFi module, and finally falls into sleep. When the set sleep time ends, it repeats the above steps again. When sleeping, if data packets sent by other wireless nodes are received, then it reads the data packets to determine whether they are consistent with the conditions. If so, it transmits the data packets, otherwise discards them.

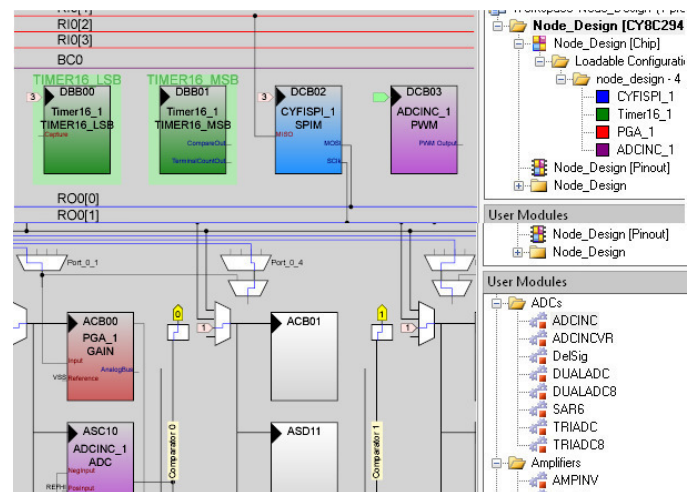


Figure 4: PSoC user module's placement and routing

Figure 4 shows a snap shot of PSoC developer IDE. This is used for PSoC-1 family. Higher family devices, i.e. PSoC 3 to 5 require PSoC Creator IDE. These IDE are different because of their different architecture of core CPU and related compiler issues. Internal block shown in figure 4 is the mixed array block. It is either digital or analog. These are most

flexible, just is like FPGA. These blocks can reconfigure as per the component required (like ADC, DAC, Counter, Timer, PGA etc). This block can be filled by the user module (pre define code for different functions by Cypress library). It has all types of user module right from programmable gain amplifier, instrumentation amplifier, to low pass, band pass filter and so on. These user modules can occupy the appropriate blocks either digital or analog or both. These features are also available in PSoC creator IDE but look wise, it is different. This entire design work bench has the flexibility in routing for input, output and internal connection between blocks. That is the reason, why in this architecture, the pin compatibility between various devices and packages is not an issue. The key pins like power and reset are computable as per the package. All the i/o functions require pinsto be defined by the user.

WSN gateway needs to read commands from the computer through the serial or USB ports and forward the commands. At the same time it even transmits the data packets sent by the wireless sensor nodes to the computer management software through the serial or USB ports, in order to facilitate the data management.

After the CyFi transceiver module receives the instructions from the WSN gateway or other neighboring nodes, the network nodes will be awakened. The processor then determines node number of the instructions. If the object of the instruction is the current node, then the node begins working. Otherwise the network node will be skipped. In addition, the monitoring software also needs to manage the entire network. In general, the monitoring software receives the data WSN gateway through serial ports, completes the processing of data summary and stores the data in the database. The data can then be queried or deleted as and when required, on the basis ofnd querying of each node's working status.

V. CONCLUSION

Although there are few sensor nodes available as CTOS but none of these have this type of flexibility to improve the performance of wireless sensor node and its network. This node supports the flexibility at almost all layer of technology: from gain of the sensor signal amplifier to the frequency hopping in wireless communication channels. It does this with

the help of software control. The few nodes mentioned above are developed and are under testing with application and are just waiting for the final approved result from laboratories. This wireless sensor node and its networks has been developed in a different domain of application. But its development and application in a practical life will be perfect and comprehensive. Therefore, the design of application specific wireless sensor nodes based on the PSoC and CyFi, does good to the further research and development of Ad-Hoc sensor network, and it may as well play a significant role in the field of WSN.

REFERENCES

- [1] Sujian Zhao et al "Software Design of a Simple Wireless Sensor Network System Based on CC2430" Wireless Communications, Networking and Mobile Computing (WiCOM), 2011 7th IEEE International Conference. PP 1-4 2011.
- [2] Sham P Nayse, Mohammad Atique, Anita Agrawal et al, "Power Aware Wireless Sensor Node Design Using PSoC" International Journal of Innovative Research in Science, Engineering and Technology Vol. 2, Issue 4 PP 1178-1182, April 2013.
- [3] El Kateeb, A. et al, "Wireless Sensor Nodes Processor Architecture and Design" Advanced Information Networking and Applications – 2nd IEEE International Conference. PP 892 – 897, 2008
- [4] Ching-Wen Chen et al, "Design of a Low-Power and Low-Latency MAC Protocol with Nodes Grouping and transmission Pipelining in Wireless Sensor Networks; PP 143 - 147 2008
- [5] Bo Chen ; Tomizuka, M. "Open Architecture Design of Structural Health Monitoring Software in Wireless Sensor Nodes" Mechtronic and Embedded Systems and Applications, International Conference PP 19 - 24 2008.
- [6] Feng Tian ; Xiaowu Xu "Design of Wireless Sensor Networks Node in Coalmine" Intelligent Computation Technology and Automation, Second IEEE International Conference, Vol. 4 PP 66 - 69 2009.
- [7] Dzung, D. et al, "Design and implementation of a real-time wireless sensor/actuator communication system" Emerging Technologies and Factory Automation, 10th IEEE Conference Vol.2 PP 442-2005
- [8] Sasilatha, T. ; Raja, J. "Design and analysis of a 1.2V, 2.4 GHz Low Power ASK Transmitter for Wireless Micro Sensor Nodes" Wireless Communication and Sensor Networks, Third International PP 17 - 20 , 2007
- [9] Daboli, A. et al; "Dynamic reconfiguration in a PSoC device",. FPT IEEE International Conference PP 361-363, 2009
- [10] Data sheet and technical manual Cypress Inc.