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The multi-topology converter for the solar panel

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***Abstract*—In this paper, we propose voltage converter with high efficiency over wide input voltage. This converter is suitable for the solar panel for WSN applications where the only power source is a solar cell that outputs highly variable voltage. The aim is to achieve this by using multiple converter topologies in parallel. Use of such converter has a meaning in renewable resources that in the long term operation significantly change their output voltage. The efficiency of particular topologies is estimated in simplified loss model, which is later experimentally tested.**

I. Introduction

EFFICIENT ENERGY production from alternative sources is one of the main problems that must be solved to make the use of solar or wind power came to the fore. The greatest weakness of renewable energy sources is their fluctuating power availability [1]. Existing power converters are tuned for operation at peak power of the particular source. The task of this paper is to design a converter that can efficiently take power from renewable source even while their energy potential is lower. To do this we need to examine the efficiency of commonly used topologies to determine their suitable operating point. This would allow creating control unit able to operate multiple topologies in parallel while maintaining better total efficiency than single topology converter.

II. The model of topologies

There are multiple topology designs for DC-to-DC converters. This paper will consider topologies with potentially lowest power loss, disregarding their other properties (output noise, transient response, etc.). Favorable candidates are elementary step-up and step-down converters (Fig. 1 and 2). They contain least components and offer relatively high efficiency while V_{in}/V_{out} ratio is close to one [2]. Harvestable power sources, however, offer a wide range of operating voltage. In such cases, other topologies may be preferable. Effective conversion with high V_{in}/V_{out} difference is a convenient property of transformers. Integrating transformer into mentioned topologies will result in fly-back transformer converter (Fig. 3) [3].

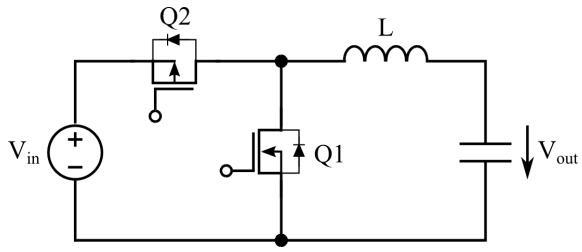

Fig. 1. Step-down converter basic topology

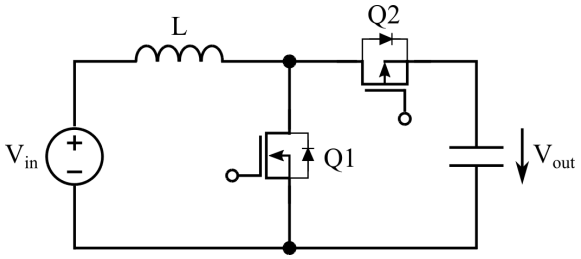

Fig. 2. Step-up converter basic topology

Our application for sensor nodes assumes solar cell as a power source. This means an available voltage will heavily fluctuate from low during dawn and dusk to high during midday. To find out which topology is most effective for given input voltage we need a model of losses for each of them. Simplified loss model of buck and boost converters can be described as shown in equation 1. Loss of the two topologies differentiate by RMS current calculation of particular branches. Table I contains the list of squared currents with their respective duty cycle D, where I_{RMS_L}, $I_{RMS_{Q2}}$ and $I_{RMS_{Q1}}$ represent effective current through inductor and transistors respectively [4].

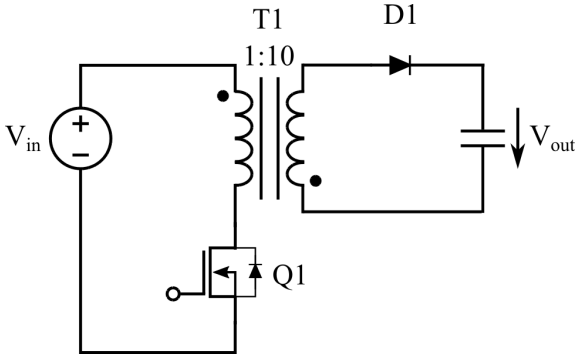

Fig. 3. Fly-back transformer topology

TABLE I
COMPUTATIONS OF CURRENTS WITH RESPECT TO THE DUTY CYCLE

	I_{RMS_L}	$I_{RMS_{Q2}}$	$I_{RMS_{Q1}}$
Buck	I_{out}^2	$I_{out}^2 \cdot D$	$I_{out}^2 \cdot (1-D)$
Boost	$(\frac{I_{out}}{1-D})^2$	$(\frac{I_{out}}{1-D})^2 \cdot (1-D)$	$(\frac{I_{out}}{1-D})^2 \cdot D$

$$\begin{aligned} P_{loss} = {} & R_{DS(ON_{Q1})} \cdot I_{RMS_{Q1}} + Q_G \cdot V_{G_{Q1}} \cdot f + \\ & \frac{1}{2} V_{IN} \cdot I_{RMS_{Q1}} \cdot (\frac{Q_G}{I_G} + \frac{Q_G}{I_G}) \cdot f + \\ & R_{DS(ON_{Q2})} \cdot I_{RMS_{Q2}} + Q_G \cdot V_{G_{Q2}} \cdot f + \\ & R_L \cdot I_{RMS_L} \end{aligned} \tag{1}$$

where:

- $R_{DS(ON_{Q1})}$ - drain-source resistance of transistor Q_1
- Q_G - total gate charge
- V_G - gate voltage (same as output voltage)
- I_G - gate charge current
- R_L - inductor resistance at switching frequency
- f - switching frequency

Power loss in the fly-back circuit can be approximated as stated in equation 2 [5]. This loss model simplifies transformer loss only to its wiring loss. Core loss is omitted due to the anticipation of low power provided by solar cell during operation of this topology.

$$\begin{aligned} P_{loss} = {} & R_{DS(ON_{Q1})} \cdot I_{RMS_{Q1}} + Q_G \cdot V_{G_{Q1}} \cdot f + \\ & \frac{1}{2} V_{IN} \cdot I_{RMS_{Q1}} \cdot (\frac{Q_G}{I_G} + \frac{Q_G}{I_G}) \cdot f + \\ & R_{L1} \cdot I_{RMS_{L1}} + R_{L2} \cdot I_{RMS_{L2}} + \\ & V_{D1} \cdot I_{RMS_{D1}} \end{aligned} \tag{2}$$

where:

- R_{L1} - primary winding at f
- R_{L2} - secondary winding at f
- V_{D1} - diode forward voltage drop

Duty cycle computation for boost and fly-back topologies is described in equation 3 and 4 respectively [6].

$$D = 1 - \frac{V_{in}}{V_{out}} \tag{3}$$

$$D = \frac{\frac{V_{out}}{V_{in}}}{\frac{N_s}{N_p} + \frac{V_{out}}{V_{in}}} \tag{4}$$

A. Optimal operating point

Next step is to fill described models with parameters of real-world equipment measured at switching frequency (Tab. II). We have chosen components that will later be used for testing. However, these components are by no means ideal for the power converter, which will be reflected in converter's efficiency [7].

We will simulate load at 3.3V drawing 10mA constant current. To minimize unaccounted parasitic losses, we have chosen lowest operating frequency that allows continuous conduction mode of operation. Transistors will, therefore, operate at 100kHz. Figure 4 shows the efficiency of step-up topologies relative to the input voltage. The simulation shows ranges of input voltage where respective topologies achieve better efficiency than the others.

TABLE II
LIST OF COMPONENTS USED FOR THE TESTING

	Component
N-channel MOSFET	TN0604N3
P-channel MOSFET	LP0701N3
Inductor	Generic toroid coil
	L = 203uH R=5.35 OHM
Diode	IN5817
Transformer	Rp=1.16 OHM, Lp = 51.9uH
	Rs= 33.6 OHM, Ls = 5.116mH
	Turn ratio 1:20

III. DESIGN OF MULTI-TOPOLOGY CONVERTER

Utilizing optimal operating point given by particular topology can be achieved by power management system with multiple parallel topologies and suitable control algorithm. The parallel conjunction of buck and boost topologies require some modifications [8]. Main reason is body diode of switching transistors. In the case of boost topology (Fig. 2), body diode

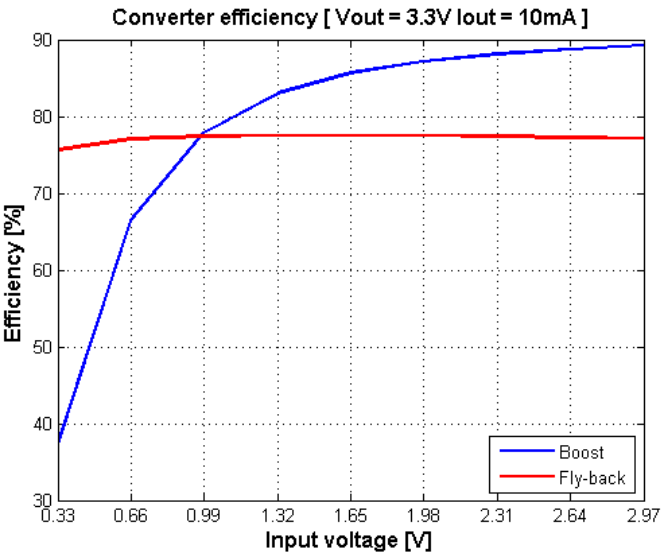

Fig. 4. Converter efficiency

of $Q2$ restricts the use of input voltage to value lower than the output voltage. If this restriction is not respected, body diode will conduct current making it impossible to maintain regulation on the output voltage. The similar limitation can also be observed on buck topology when the output voltage is greater than the input. This raises a need to add an extra transistor, which would be controlled to restrict current in cases where body diode is conductive. The more convenient solution is to add not one, but two transistors resulting a buck-boost topology where input and output voltages are separated by two transistors (Fig. 5). This modification will increase overall power loss due to extra resistance of constantly opened transistor - $R_{DS(ON)}$ of P-channel transistor.

This way, the properly designed control algorithm can step-up or step-down input voltage regardless of V_{in}/V_{out} ratio. Control signals needed for operation are described in Tab. III.

Choice of topologies and their total number depends on the used power source. For WSN node with a low power solar cell, we have chosen one fly-back and one buck-boost topology. For more power demanding appliances and sources it may be beneficial to have multiple buck-boost topologies due to the decrease of conductive losses [9]. Schematic of resulting converter for a solar cell is shown in figure 6.

IV. Experimental testing of the model

Verification of loss model will be performed on designed converter in boost operating mode. The converter will be tested for efficiency at the constant output voltage and current with a variable input voltage. Measured results are compared with loss model in Tab. IV.

Measurement confirms modeled data within an acceptable margin of error. As model estimated, this converter performs poorly while there is large difference between the input and the output voltage. This is due to high conduction losses that contribute about 90% of the total loss. Main reason is properties of used testing components. Better overall efficiency can be achieved by balancing conduction losses with switching losses (i.e. using transistors with lower drain-source resistance at cost of higher gate charge).

TABLE III
Control signals description

	Inactive	Boost	Buck
Q1	High / closed	Low / open	Switching at D
Q2	High / closed	Switching at (1-D)	Low / open
Q3	Low / closed	Low / closed	Switching at (1-D)
Q4	Low / closed	Switching at D	Low / closed

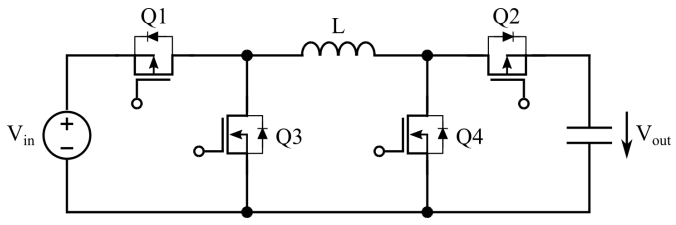

Fig. 5. Buck-boost topology

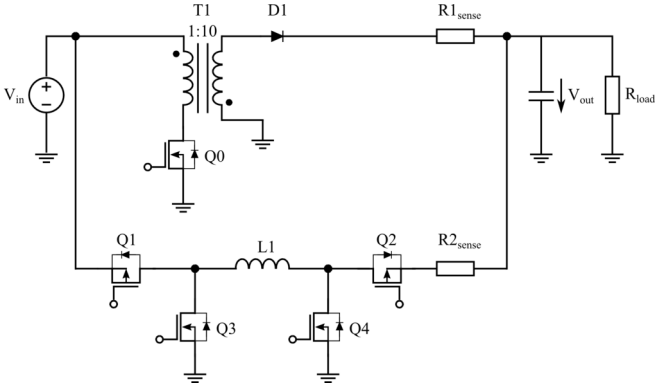

Fig. 6. Schematic of resulting converter for a solar cell

TABLE IV
Modelled and measured efficiency comparison

Input/output voltage ratio [%]	Modeled efficiency [%]	Measured efficiency [%]
10	37.32	34.81
20	66.44	65.10
30	77.90	75.94
40	82.99	81.73
50	85.63	84.33
60	87.16	85.64
70	88.12	87.60
80	88.77	88.05
90	89.22	88.67

This paper, however, shows relative efficiency between two voltage increasing topologies. The efficiency of both, boost and fly-back topologies can be improved with technologically advanced components. The elementary shape of their efficiency to input voltage function should, however, remain similar, which is given by topology operation. With boost topology, a high difference between input and output affects duty cycle. High duty cycle means a long time to charge inductor and a short time to discharge it. This creates high current peaks and therefore a significant loss. The fly-back converter may use transformer ratio to cope with high voltage difference and keep duty cycle in balance. This can also be seen from the computation of their respective duty cycle (Eq. 3 and 4).

V. Conclusion

We have evaluated voltage converter which utilizes multiple parallel topologies. Modeled data shows convenience of parallel operation of different topologies. As a result, fly-back and boost topologies are well suited for complementary operation where fly-back will be active at the lower input voltage and boost at higher. We also develop control algorithm selecting best available topology for devices with low computational power.

Implementation of modeled data into converter control may have a form of the lookup table where the device would measure all relevant parameters (input and output voltage, output current and current passing each active topology) and decide which topology (or their combination) to use. Experimental measurement confirmed our expectations about the efficiency of single topology derived from the model. To perfect efficiency for wider operating conditions, more topologies need to be examined.

REFERENCES

[1] M. Kochláň et al, "Control unit for power subsystem of a wireless sensor node", in *FedCSIS proceedings of the 2015 Federated conference on Computer science and information systems*, 2015, pp. 1249-1256, ISBN 978-83-60810-65-1.

[2] Mohan, Undeland and Robbins, "Power Electronics, Converters, Applications and Design." 2nd edition Wiley. ISBN 0–471–58408–8.

[3] R. D. Middlebrook and S. Cuk, "A General Unified Approach to Modeling Switching-Converter Power Stages", in *International Journal of Electronics*, Vol. 42, No. 6, pp. 521-550, June 1977.

[4] AN707, "Designing a High Frequency, Self–Resonant Reset Single Switch Forward Converter Using Si9118/Si9119 PWM/PSM" in *http://www.vishay.com/document/70824/70824.pdf*.

[5] AN1114, "Switch Mode Power Supply (SMPS) Topologies (Part I)" in *http://ww1.microchip.com/downloads/en/AppNotes/01114A.pdf*.

[6] AN607, "DC-to-DC Design Guide" in *http://www.vishay.com/docs/71917/71917.pdf*.

[7] G. W. Wester and R. D. Middlebrook, Low-Frequency Characterization of Switched Dc-Dc Converters, in *IEEE Transactions an Aerospace and Electronic Systems*, Vol. AES-9, pp. 376-385, May 1973.

[8] G.A. Rincón-Mora, Power Management ICs - A Top-Down Design Approach, ISBN: 1-4116-6359-4.

[9] M. Gildersleeve, G.A. Rincón-Mora et al, "A comprehensive power analysis and a highly efficient, mode-hopping DC-DC converter," in *IEEE Asia-Pacific Conference on ASIC*, 2002, pp. 153-156.