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# Real-time controller design based on NI Compact-RIO

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***Abstract*—The paper is focused on NI Compact-RIO configured as a controller for the active magnetic levitation used here as a benchmark for time-critical systems. Three real-time configurations: soft, soft with IRQ and hard FPGA are considered. The quality of the real-time control has been tested for each configuration.**

***Index Terms*—real-time control, magnetic levitation, CompactRio, scheduling.**

## I. Introduction

THREE different NI Compact-RIO (cRIO) configurations are designed and verified in control experiments performed in the real-time. The main attention is focused on real-time deterministic behavior of the PID controller constructed in a different way for a particular configuration. cRIO is recommended and promoted by National Instruments company as a rugged industrial control and acquisition system that incorporates a real-time processor and reconfigurable FPGA for reliable stand-alone embedded applications. The active magnetic levitation used here as a benchmark is a time-critical system. Therefore, a punctual and fully determined control algorithm is required. The quality of the control algorithm execution depends strongly on a used platform: Power PC or FPGA and the execution mode: software timing loop, interrupt event, hardware timing loop. A desirable design goal is usually the construction of the so-called "hard real-time" system. We do not always manage to meet this goal. In principle, to develop the hard real-time controller a certain level of familiarity with cRIO and skill is required. Control experiments that have been performed illustrate several timing aspects: jitter, execution time of control algorithm, determinism of data exchange, ect. It is important to answer to the following question. How far one can dimnish the sampling period not disturbing the system performance?

## II. Real-Time Control Application Design

The reconfigurable control system may contain the following components:

1) cRIO FPGA core application for input, output, communication, and control,
2) time-critical loop for floating-point control, signal processing, and point-by-point decision making
3) normal-priority loop for embedded data logging, remote Web interface, and Ethernet communication
4) networked host PC for remote graphical user interface, historical data logging, and postprocessing

Depending on requirements of an application, one can implement particular components. The RIO FPGA chip is connected to the I/O modules in a star topology, for direct access to each module for precise control and unlimited flexibility in timing, triggering, and synchronization. A local PCI bus connection provides a high-performance interface between the RIO FPGA and the real-time processor. The magnetic levitation control system structure is shown In Fig. 1.

A PC is dedicated to data acquisition and monitoring. The cRIO-9014 controller is equipped with two hardware platform: the Power PC microcontroller operating under the real-time the VxWorks operating system and FPGA (a Spartan-3 XILINX chip containing 3 milions gates). Power PC is triggered by a 400 MHz clock. FPGA is triggered by a 40 MHz clock. The PWM generator of the control signal is implemented in FPGA. There are also two modules: NI 9401 digital I/O and NI 9215 analog I/O. The PWM signal is transfered from FPGA through the NI 9401 output digital module and the PWM power interface to the electromagnet that operates as the actuator. The signal proportional to the sphere position is transfered from the sensor to the sensor conditioning circuit and farther to the NI 9215 input analog module.

## III. Time-critical experiments of two cRIO configurations

Three cRIO configurations shown in Fig. 2 have been built to be tested:

1) Power PC soft real-time,
2) Power PC Interrupt ReQuest (IRQ),
3) FPGA hard real-time.

The PID controller operating in a hard real-time loop is built inside the FPGA chip (Fig. 3). The sampling period can be changed.

However, its minimal value has to be set to 10 ms due to the conversion time of the analog signal (the maximal value is equal to 100 kHz per chanel). The real-time platform is responsible for communication with FPGA and the application that runs on PC and is responsible for changing the parameters of the generator PWM and PID controller. If we use Power PC and VxWorks as a real-time control platform then FPGA is only used to receive the measurment signal and transfer the control signal and measure the so-called jitter signal. The timing loop operating at the 40 MHz frequency is responsible for generating the PWM resolution signal. It generates also the 32-bits counter (in ticks) for the jitter measuring. The measurement accuracy is the clock triggering frequency dependent and is equal to 25 ns. The time-critical while loop executes the PID control algorithm. The position signal related to the sphere position is scaled in meters due to the one-dimensional

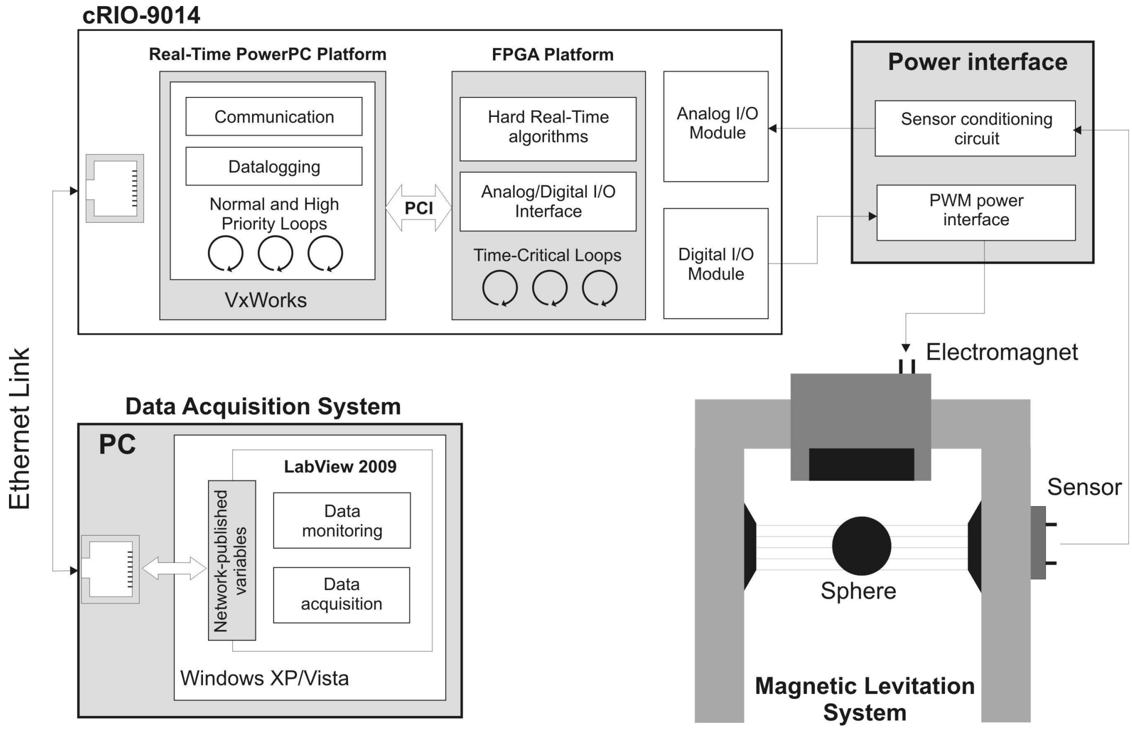


Fig. 1. Structure of magnetic levitation control system

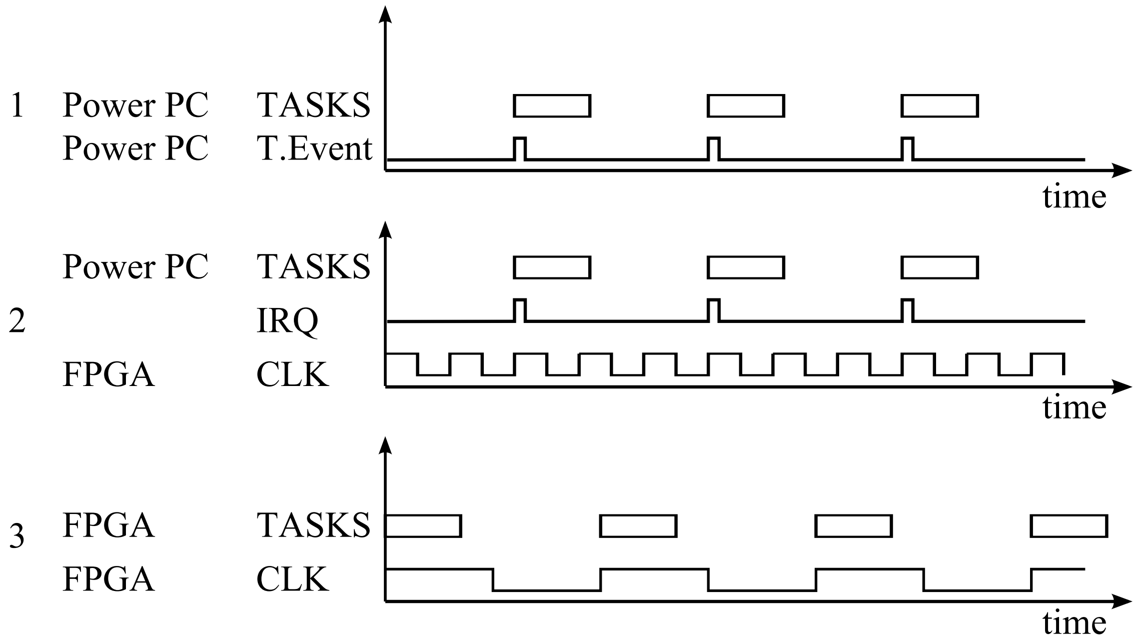


Fig. 2. Three experimental cRIO configurations

look up table. Calculations of the controller are expressed as fixed-point numbers wit the accuracy equal to $1.5259 \cdot 10^{-5}$. The output signal of the controller is a number from the range $0 \div 1$. It is scaled and becomes a duty cycle in the range $0 \div 4095$ as far as the 12-bits resolution is concerned. The sampling period for the FPGA hard real-time configuration has been verified and the 25 ns value has been confirmed. This is obvious due to the hardware paralel implementation of the PID algorithm. In Fig. 4 the logging sessions of primary work parameters corresponding to the operational VxWorks system (the upper frame) and to the realization of the user application (the lower frame) are shown. During the Power PC

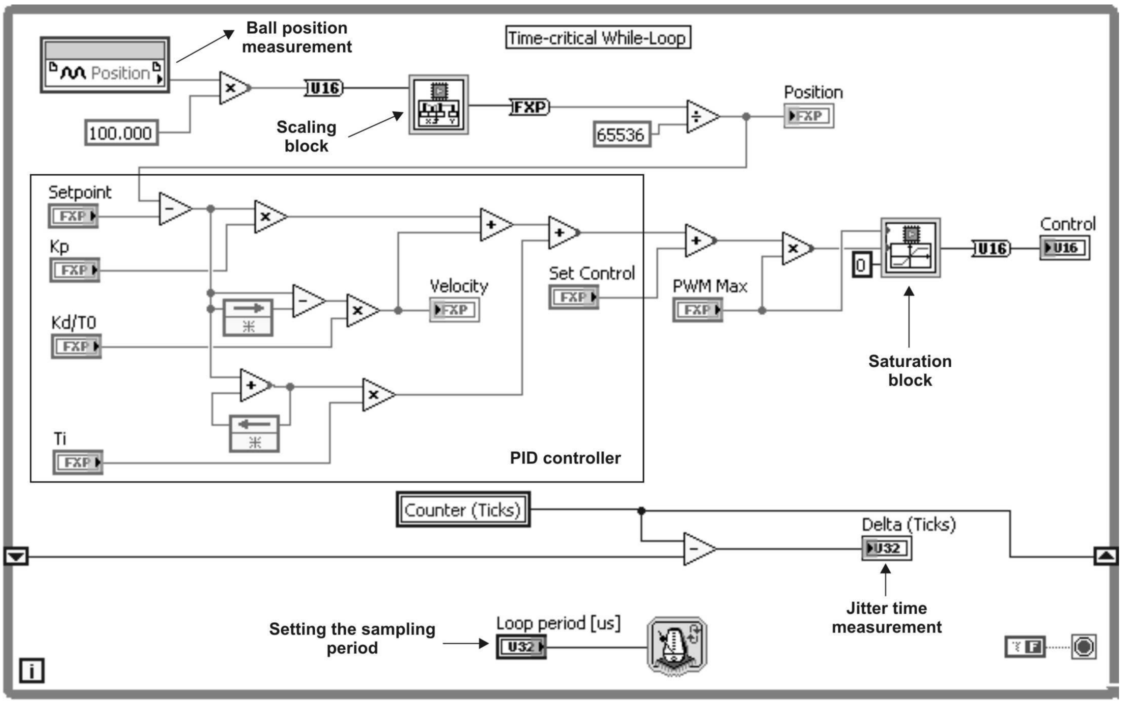


Fig. 3. The PID controller operating in a hard real-time loop running on FPGA chip

session calculation procedures have been executed with data exchange with the FPGA system. This was done to check the performance of this platform with the overhead time devoted to communication. The grey area in Fig. 4 corresponds to one complete execution of the loop which lasts 1 ms. Four interesting signals can be noted in the lower frame, namely: 0-SquareGener, 1-PositionScale, 2-PD_Controller, 4-Saturation. The first one provides square wave signal generator. The second one is devoted to scaling of the sensor signal. Next one implements the PID controller and the last one limits the control signal to the physical bounds. The execution times of these procedures are 28.1334 ms, 22.8882 ms, 30.0407 ms and 16.2125 ms respectively. It means that the time of calculations together with the context switching time between the procedures is equal to 355.84 ms. Hence, the maximal theoretical sampling frequency, without taking into account VxWorks time overhead, is equal to 2.81 kHz. In practice one should not go beyond 1 kHz. Similarly to the Power PC soft real-time configuration the performance of the Power PC Interrupt ReQuest control structure was check by running the Real-Time Execution Trace Toolkit session.

In Fig. 5 the logging data are presented. As can be seen the real-time task is IRQ triggered. The PowerPC platform waits for interrupt generating by FPGA. The execution times of the calculation procedures are comparable to Power PC soft real-time configuration. However the total time of calculations is shorter (equal to 253.27 ms). Hence, the maximal theoretical sampling frequency, without taking into account VxWorks time overhead, is equal to 3.95 kHz. In practice one should not go beyond 2 kHz.

## IV. Experimental jitter of two configurations

The real-time controllers have been tested in three cases. However, the jitter has not been illustrated in the third case. This is not a mistake. There is nothing to show. Only the third case is characterized by high accuracy and repeatability of execution determined by 25ns resolution. The FPGA chip is triggered by the hardware timer. In contrast to this case, the first two have different triggering mechanisms. Usually, they introduce uncertainty into the real-time execution. The time stamps in the number of control task events 650 were registered for jitter analysis. The histograms are scaled in the full range of the available data. The results corresponding to two experimental cRIO configurations (see Fig. 2) are shown in Fig. 6 and Fig. 7. Let us define the following factors for further results analysis:

- min - is the minimal time instant registered for an event,
- max - is the maximal time instant registered for an event,
- N - is the maximal number of requests at the same time interval.
- xs [$\mu$s] - is the time instant related to the maximal number of events, alas different to the nominal (desired) time instant,
- DN [%] - is the negative deviation from xs,
- DP [%] - is the positive deviation from xs,
- DNn [%] - is the negative deviation from the nominal (desired) time instant,
- DPn [%] - is the negative deviation from the nominal (desired) time instant.

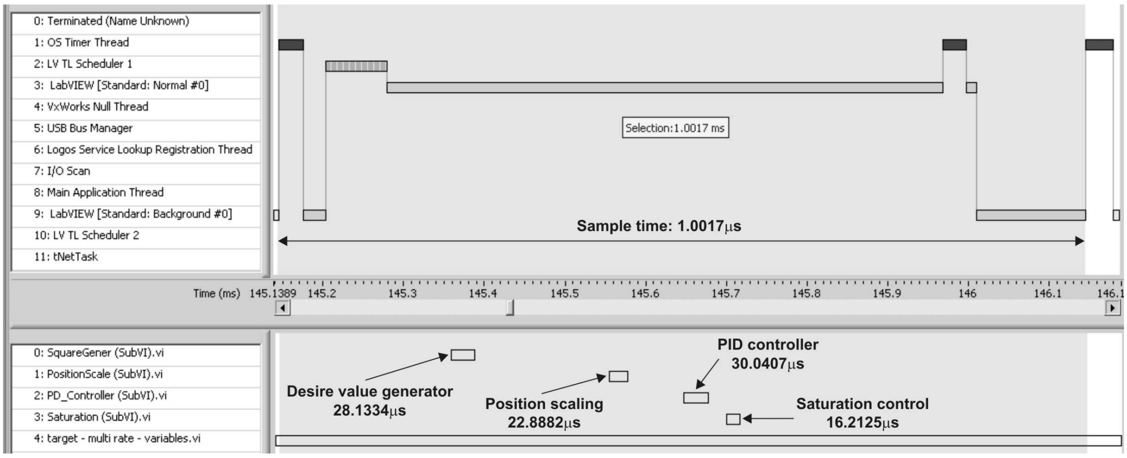


Fig. 4. Real-Time Execution Trace Toolkit session for the Power PC soft real-time configuration with 1 ms sample period

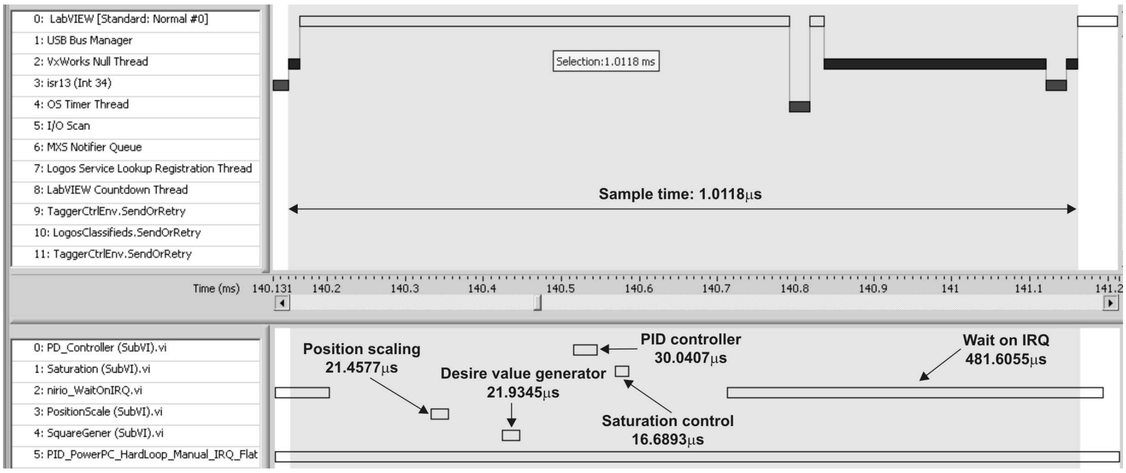


Fig. 5. Real-Time Execution Trace Toolkit session for the Power PC Interrupt ReQuest configuration with 1 ms sample period

### A. Configuration 1

One can notice that the sampling frequency equal to 1 kHz is a critical value for the soft real-time. Decreasing the sampling period (from 1 ms to 0.5 ms) is not feasible. The system operates at 995 ms (see Fig. 6c). This demonstrates that the clock mechanisms used by LabView and VxWorks do not cooperate correctly in the Power PC timing loop configuration. Moreover this environment shows also a lack of punctuality for 1 and 2 ms sampling periods (see the histograms in Fig. 6a and Fig. 6b).

TABLE I
STATISTICS OF CASE 1

| Case | min [$\mu$s] | max [$\mu$s] | N |
|---|---|---|---|
| a | 1976.847 | 2065.452 | 99 |
| b | 1083.259 | 1116.691 | 36 |
| c | 963.333 | 1026.092 | 80 |

In the case of timing events triggered by the FPGA clock. when tasks are executed at Power PC (illustrated in Fig. 7)

TABLE II
CONFIGURATION 1 CASE A

| | |
|---|---|
| xs | 2005.788 |
| DN % | -1.442 |
| DP % | 2.974 |
| DNn % | -1.157 |
| DNp % | 3.272 |

TABLE III
CONFIGURATION 1 CASE B

| | |
|---|---|
| xs | 1098.379 |
| DN % | 1.376 |
| DP % | 1.667 |
| DNn % | 8.325 |
| DNp % | 11.669 |

we are also surprised by the fact that the system triggered by the FPGA interrupt responds in a strange way. There is a large distribution of single events fortunately quantitatively

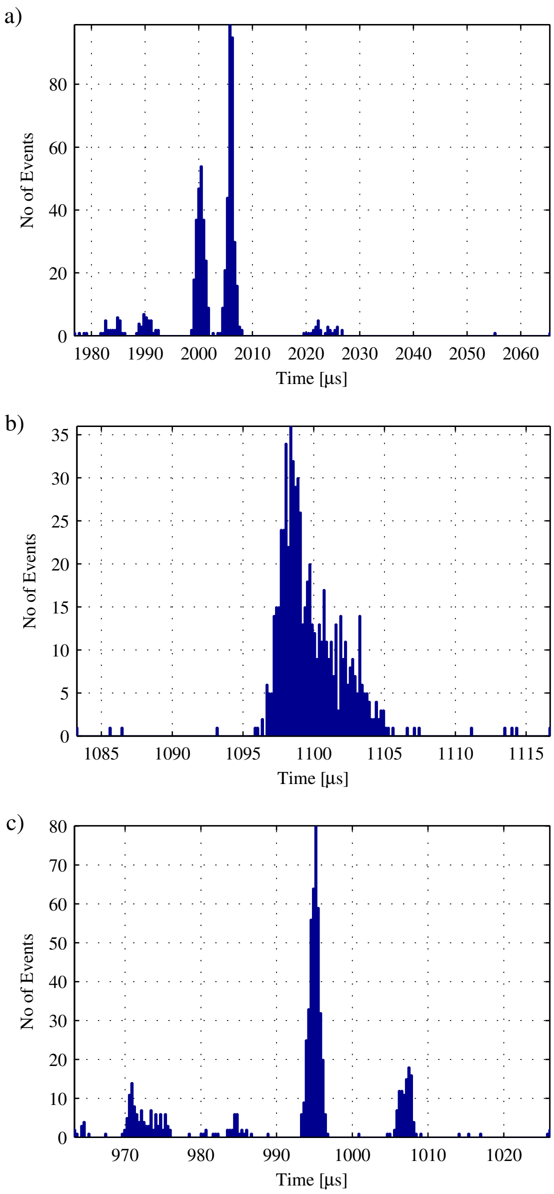


Fig. 6. . Histograms a) 2ms, b) 1ms, c) 0.5 ms for the timing loop with the time critical priority.

TABLE IV
CONFIGURATION 1 CASE C

| | |
|---|---|
| xs | 995.185 |
| DN % | 3.200 |
| DP % | 3.105 |
| DNn % | 92.666 |
| DNp % | 105.218 |

insignificant. It is surprising, as if the interrupt handler poorly managed IRQ despite the existence of the acknowledgment mechanisms. Of course, one could neglect the events that occurred fewer times than 10% of the 650 recorded events. Then statistics would be beneficial for the IRQ. As far as Configuration 2 is concerned we can notice a significant improvement in control quality, much of the tasks is executed in the vicinity of the desired time. However, even at such a small number of events as 650 there was a significant time variation (jitter) resulting from the interrupt handler (interrupt routines).

### B. *Configuration 2*

Analysing the collected data it should be noted that in both cases (the Configurations 1 and 2), the magnetic levitation system steered by PID controller, where the derivative of the error is determined, would pay a high risk of loss of stability in the worst case, at best, the occurrence of oscillations. Uneven course of events has influence on the rate of change of the error signal fed to the input of the differentiating controller part. Unfortunately, a value calculated in such a way is incorrect and inconsistent with reality.

TABLE V
STATISTICS OF CASE 2

| Case | min [$\mu$s] | max [$\mu$s] | N |
|---|---|---|---|
| a | 1791.058 | 2490.667 | 353 |
| b | 723.133 | 1214.041 | 410 |
| c | 373.309 | 645.915 | 105 |

TABLE VI
CONFIGURATION 2 CASE A

| | |
|---|---|
| xs | 2005.510 |
| DN % | 10.693 |
| DP % | 24.191 |
| DNn % | 10.447 |
| DNp % | 24.533 |

TABLE VII
CONFIGURATION 2 CASE B

| | |
|---|---|
| xs | 999.423 |
| DN % | 27.644 |
| DP % | 21.474 |
| DNn % | 27.686 |
| DNp % | 21.404 |

TABLE VIII
CONFIGURATION 2 CASE C

| | |
|---|---|
| xs | 499.338 |
| DN % | 25.239 |
| DP % | 29.354 |
| DNn % | 25.338 |
| DNp % | 29.183 |

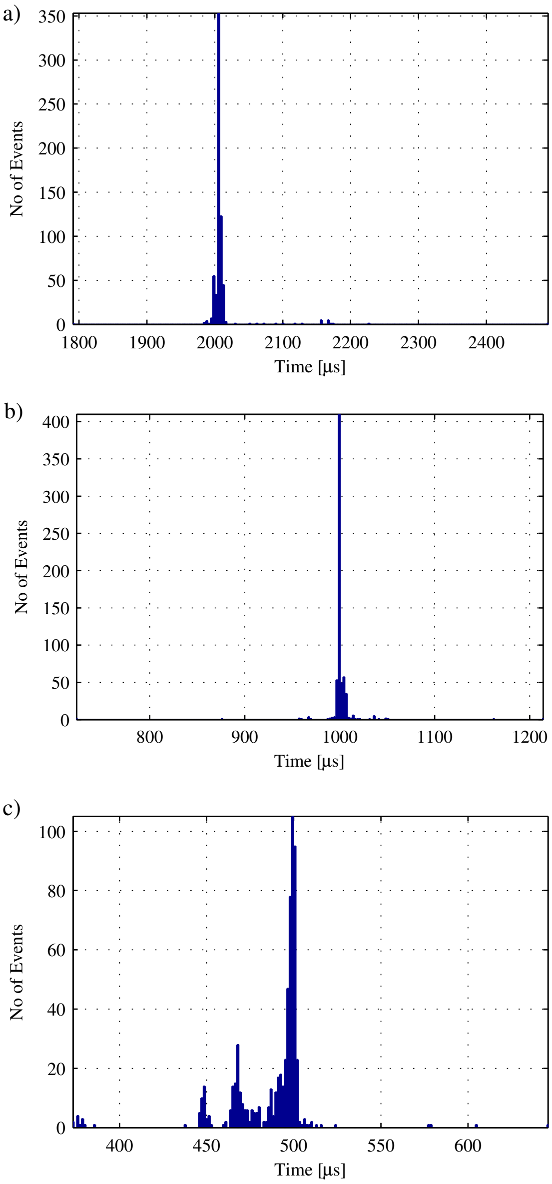


Fig. 7. Histograms a) 2ms, b) 1ms, c) 0.5ms for IQR timing events triggered by the FPGA clock. Tasks executed at Power PC

## V. Conclusion

With this research it has been shown that the real-time control development must be considered precisely and with specific attention to the used hardware. The designed controller must be checked and verified how operates. Especially the punctuality of the control task call must be satisfied. The timing loop mechanism with time-critical priority is a fine mechanism for triggered tasks, but is limited to 1kHz of the sampling frequency. The timing events are condensed around the requested sample period. In the case of IRQ driven task, generated on the base of FPGA clock, the events are handled at the desired sample time, but sometimes a few events are called with a distance of about 25% far away from the nominal trigger time. The observed jitter gives a number of inequalities in the controller calculation. Note, that the error derivative calculation is very sensitive for incorrect timing. The tested National Instruments CompactRIO hardware gives a number of possibilities to develop a wide range of control configurations. The PowerPC is dedicated to data management and exchange between hard time-critical layer realised in the FPGA. Summarising, the control task should be implemented in the FPGA and the Power PC used for data acquisition and controller adjustment task only.

## References

[1] P. Bilik, L. Koval and J. Hajduk, *CompactRIO Embedded System in Power Quality Analysis*, Proceedings of the International Multiconference Computer Science and Information Technology, 2008, pp. 577 580

[2] W. Blokland and G. Armstrong, *A CompactRIO-based Beam Loss Monitor for the SNS RF Test Cave*, Proceedings of EPAC08, Genoa, Italy, pp. 1050-1052

[3] C. Dase, J. S. Falcon, and B. MacCleery, *Motorcycle Control Prototyping Using an FPGA-Based Embedded Control System*, IEEE CONTROL SYSTEMS MAGAZINE October 2006, pp.17-21

[4] InTeCo Ltd., *Magnetic Levitation System, Users Guide*, Inteco 2003

[5] National Instruments LabVIEW Toolkit Web portal, "LabVIEW Toolkits," [Online]. Available: http://www.ni.com/toolkits

[6] National Instruments LabVIEW Real-Time Web portal, "LabVIEW Real-Time for measurement and control," [Online]. Available: http://www.ni.com/realtime

[7] A. Pilat, *Control of magnetically levitated systems*, Ph.D. Dissertation (in Polish), AGH University of Science and Technology, 2002, Kraków, Poland