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SENTIOF: An FPGA Based High-Performance and Low-Power Wireless Embedded Platform

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***Abstract*—Traditional wireless sensor nodes are designed with low-power modules that offer limited computational performance and communication bandwidth and therefore, are generally applicable to low-sample rate intermittent monitoring applications. Nevertheless, high-sample rate monitoring applications can be realized by designing sensor nodes that can perform high-throughput in-sensor processing, while maintaining low-power characteristics. In this paper, a high-performance and low-power wireless hardware platform is presented. With its compact size and modular structure enabling there to be an integrated customized sensor layer, it can be used for a wide variety of applications. In addition, the flexibility provided through dynamically configurable interfaces and power management, helps optimizing performance and power consumption for different applications.**

***Keywords*—FPGA, wireless platform, high-throughput, low-power**

I. Introduction

With the advent of low-cost, low-power, and miniature size electronics, wireless sensor nodes have emerged as a low-cost alternative to fixed wired-based sensing solutions. These nodes are typically designed using a low-power micro-controller, a radio transceiver, and one or more sensors to measure a particular physical phenomenon. Based on the limited computational performance, communication bandwidth, and lifetime, these nodes have traditionally been applied to particular low-sample rate intermittent monitoring applications in different field [1]-[4]. However, their potential advantages have provided the motivation to explore them in relation to high-sample rate applications.

Given the limited bandwidth and high-power consumption of radio transceivers that are typically used in these nodes, the major challenge lies in transmitting a large amount of data generated by high-sample rate applications. In order to overcome this challenge, researchers have proposed in-sensor processing [5]-[8] in which, raw data is processed locally in a sensor node, and only results are transmitted wirelessly. Therefore, it reduces communication activity and the associated power consumption. However, it is observed that typical low-power micro-controllers integrated in sensor nodes, often lack high-throughput performance when complex mathematical and signal processing algorithms are involved. Therefore, to meet the demands of high computational performance, the prototype design reported in [5] employs a high-throughput micro-controller for in-sensor data processing, in addition to a low-power 8-bit micro-controller. In [6], a Field Programmable Gate Array (FPGA) based in-sensor processing solution is demonstrated in relation to an image processing application. In [7] and [8], FPGA-based commercial evaluation kits and micro-controller based wireless nodes were used to investigate their performance and energy consumption for high-sample rate applications. Based on the presented results in these articles, it can be concluded that high-throughput processing requirements can only be fulfilled through an FPGA, however, by accurately distributing the processing, communication and control specific tasks on a micro-controller and an FPGA, it is possible to optimize both the performance and power consumption for an application.

By analyzing the published literature relating to high-performance wireless nodes, it was found that there are only two such nodes, [9] and [10] that are able be used for high-throughput in-sensor processing. Both nodes are very similar in their design, as they are built on a similar layered structure and they integrate similar modules. For example, each has a sensor layer, a processing layer consisting of micro-controller and/or an FPGA, a communication layer to enable wireless communication and, in addition, to a power supply layer. On both nodes, the processing layer consists of an FPGA that can be used for in-sensor processing. However, both these FPGAs (Spartan-IIE, and Spartan-IIIE) were built on a technology that is now a decade old and therefore, does not offer the high-performance and low-power consumption that is the case with the modern FPGAs. Apart from that, inter module communication interfaces such as between FPGA and micro-controller, and between wireless transceiver and micro-controller are fixed in these nodes and therefore, cannot be re-configured for different applications without modifying the hardware design. Additionally, the compactness of these nodes is compromised because of the extra height, resulting from the interface connectors on both sides of a layer and also stacking of four layers on top of each other to form a complete working node.

To overcome the above mentioned problems, we have developed a high-performance, low-power and compact wireless embedded platform, the SENTIOF that is shown in Fig. 1. It integrates a micro-controller, an FPGA, an SRAM, a FLASH, and a radio transceiver on a single printed circuit board (PCB), while providing easy integration of a customized sensing layer,

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in order to use it in different applications. The SENTIOF is designed with the following key characteristics.

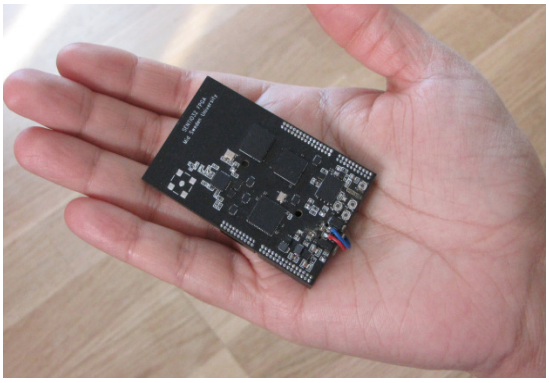

Figure 1. The SENTIOF platform

High-Performance In addition to sequential processing capabilities, there must be support for hardware acceleration in order to perform computationally intensive processing.

Low-power The integrated components should be operable at different clock frequencies so as to optimize the power consumption and performance. In addition, the platform must support a dynamic power management to switch-off unused components.

Sensor integration The platform must support easy integration of application dependent sensors. Therefore, in addition to different power supply voltages, a large number of input-output interfaces from a micro-controller and FPGA should be provided for this purpose.

Flexibility In addition to the easy integration of sensors either with a micro-controller, FPGA or both, the platform must support the easy realization of application dependent communication between the micro-controller and the FPGA.

Compact size The platform should have small dimensions so that it can be deployed in applications with space constraints.

The details regarding the design, performance and power consumption of the SENTIOF are the main focus of this paper. The remaining sections are organized as follows. Section II describes the hardware design aspects of the SETNIOF. Section III is devoted to software related details. In section IV, the performance and the power consumption analysis are presented, while concluding remarks are given section V.

II. Hardware Design

A simplified design of the SENTIOF, representing all major components and their interconnections is shown in Fig. 2. With the exception of power source, all other components are integrated in the SENTIOF platform, which is discussed in detail in the following.

A. Plateform Components

Based on the functional description of the integrated components, the SENTIOF can be divided into different logical units, such as processing, communication, memory, power management and sensor interface, and can be then described accordingly.

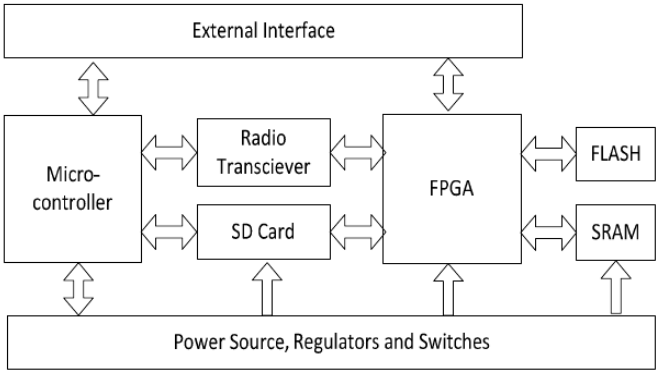

Figure 2. Architectural depiction of the SENTIOF

Processing Unit

In order to achieve a high-computational performance, two processing resources, a 32-bit micro-controller ATUC3B0512 [11], and a Spartan-6 FPGA XC6SLX16-2CPG196 [12], are integrated in the SENTIOF.

The micro-controller provides high computational capabilities by means of a compact single-cycle instruction set including DSP instructions and an operational clock frequency of up to 60 MHz. Additionally, it includes an extensive set of input-output (IO) interfaces and a number of low-power modes in order to optimize the power consumption for an application. The micro-controller can be used to process the application data, read the sensor's data, and/or communicate with the radio transceiver in order to transmit or receive data/results. In addition to its application dependent data processing, the micro-controller performs all the control specific operations such as power and FPGA configuration management and therefore, acts as a central control unit in the SENTIOF.

The micro-controller can be used as the main processing unit for a wide variety of monitoring applications. However, in order to achieve a high-throughput computational performance as required in many high-sample rate applications, the FPGA is integrated into the SENTIOF. Due to hardware parallelism, it is possible for multiple independent tasks to be realized using dedicated hardware logic in the FPGA, which thus be performed simultaneously at high speed. In addition, the re-configurability of the FPGA allows synthesizing different algorithms with optimized control and data paths, without modifying any real hardware. The selected FPGA is enriched with sufficient amount of basic logic cells, in addition to other resources such as block RAM, multiply-and-accumulator (MAC) units, and PLLs. A summary of these resources is given in Table I.

Radio transceiver

In order to enable wireless communication in the SENTIOF, an IEEE 802.15.4 compliant low-power radio transceiver, CC2520 [13] is integrated in the design. The

transceiver operates at the 2.4 GHz license free band and provides a maximum throughput of 250 kbps. In addition to 6 reconfigurable GPIOs for optional command and interrupt signals, the radio transceiver includes a SPI interface to communicate and exchange data either with the micro-controller or with the FPGA. The interface to both the micro-controller and the FPGA is achieved by means of multiplexer/de-multiplexer switches and is therefore, able to be configured dynamically. This additional flexibility can be exploited to optimize the performance and the power-consumption of the communication activity according to the requirements of an application.

TABLE I.
A SUMMARY OF LOGIC RESOURCES OF THE SPARTAN-6 FPGA XC6SLX16-2CPG196

Logic Cells	LUT size	Dis-tribu-ted RAM	Block RAM	MAC units	PLL	Number of IOs
14,579	6-input	136 kb	576 kb	32	2	106

Memory

High-sampling rate applications generally process a large amount of raw data, and generate both intermediate and finals results that must be stored in fast memories in order to achieve a high performance. Therefore, in addition to a 96 kB of SRAM in the micro-controller and 89 kB in the FPGA, a 4 MB of additional SRAM, CY62177DV30 [14] is integrated in the SENTIOF. The low-power SRAM, interfaced with the FPGA, provides a 16-bit wide data path for read and write operations that can be performed in 55 ns.

The FPGA requires re-configuration each time it is powered-on. Therefore, a high-speed and low-power FLASH based configuration memory, W25Q64BV [15][14] is used for this purpose. The selected FLASH memory provides a rapid access rate of 85 MHz and a quad serial peripheral interface (SPI), which enables the configuration of the FPGA in the minimum time. In addition to the configuration data of 4 Mb, the 64 Mb FLASH can be used to store application data.

For long term data storage, the SENTIOF is designed to support a micro-SD card. In a similar manner to that for the radio transceiver, the interface to the SD card can also be dynamically configured either to the micro-controller or to the FPGA, as it is interfaced to both these processing units through multiplexer/de-multiplexer switches.

Power

The SENTIOF is powered by means of a single DC power source, with output voltage between 3.6V and 6V. This DC voltage is fed to the SENTIOF and is then regulated and converted to four different levels as shown in Fig. 3. In relation to these four voltages, the 1.2V regulated voltage is used to power the FPGA's core while the 1.8V is used to power the radio transceiver and the core of the micro-controller. Apart from the radio transceiver, the cores of the FPGA and the micro-controller, all other components on the SENTIOF platform are powered with 3.3V. The boost convertor that can be adjusted to provide up to 6.5V, is included for external devices/sensors that may require a higher voltage than is provided by attached DC power source, i.e. typically a 3.6V. In addition to a DC power source, the SENTIOF can also be powered through a USB interface. This provides an added advantage of continuous long term power during an application development process.

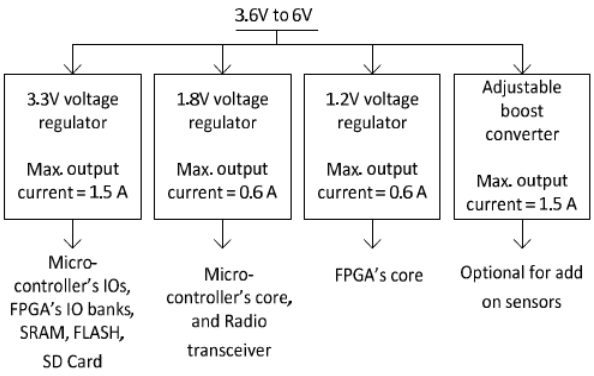

Figure 3. Power supply distribution in the SENTIOF

External Interface

The external interface provided through the 1.27 mm-pitch connectors serves three purposes. Firstly, it provides a large set of IOs, both from the micro-controller and the FPGA, in addition to all regulated power sources in order to integrate a customized sensor board with the SENTIOF. Secondly, the JTAG interfaces required to program/configure each of the micro-controller, the FPGA, and the FLASH memory from the computer are also made accessible through this external interface. Lastly, the application specific communication requirements between the micro-controller and the FPGA can also be fulfilled through this interface.

B. PCB Design

In order to ensure a high-performance and low-production cost, special consideration was given to the PCB design. This includes the separation of different ground planes, the minimization of trace length between the high-speed devices, limiting the design to a reduced number of layers, and avoiding micro and buried vias.

To minimize noise in relation to all the different types of components, four ground planes are used. A generic ground plane, GND, is used to connect ground plane of the DC power source to other planes through 0 Ohm resistors, as shown in Fig. 4. In these planes, the digital ground, DGND serves as a return path for all digital components including the FPGA, micro-controller, SRAM etc. The power ground, PGND is used to minimize the noise from other planes onto the power supply components. As there are no analog components mounted on the SENTIOF, the analog ground AGND is not used. However, it is provided to ensure that analog sensors can be reliably interfaced with the SENTIOF.

In relation to all the components mounted on the SENTIOF, it is the FPGA that has the highest pin count of 196 pins, which

are packed into 8x8 mm BGA package organized in 14 x 14 rows and columns. The 0.5 mm horizontal and vertical pin pitch resulting from this small footprint was a challenging factor, as it determined the routing and clearance rules in addition to the number of the routing layers. For example, if the manufacturer's guidelines regarding the PCB design of the FPGA [16] are strictly followed, then it requires a minimum of 7 PCB layers using micro-vias, while restricting the trace width and clearance to 0.075 mm. The production cost of the resulting PCB is then significantly higher in comparison to an equivalent PCB with a via diameter of more than 0.15 mm, and a trace width and clearance of 0.1 mm or more.

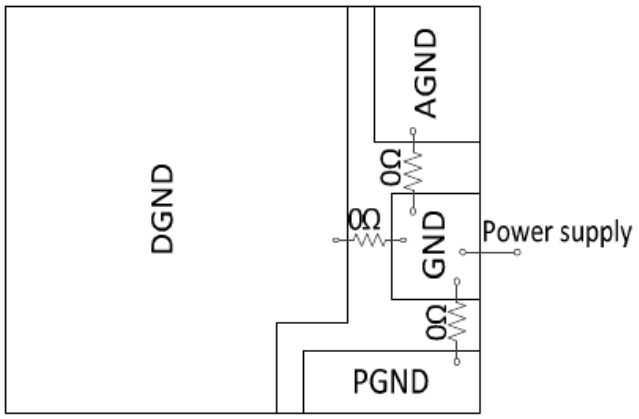

Figure 4. Ground planes used in the SENTIOF.

Therefore, to relax the production requirements, the via-in-pad option was used for the FPGA. This allowed to use larger pad size and, eventually, larger via hole diameter of 0.2 mm, a minimum trace width and clearance of 0.1 mm. In addition, it also helped to reduce the PCB design to 6 layers and without the necessity of buried vias.

Among other components, it was the radio transceiver that required the strictest observation of the manufacturer's guidelines, in order to ensure proper functionality. Therefore, the layout of the radio transceiver was completely matched with the reference layout. In addition to providing an interface for an external antenna, a PCB antenna is also incorporated for the radio transceiver.

C. Physical Structure

The size of the PCB is 65 x 40 mm, with 5 mm of interface height on one side that is used to attach a sensor module. A sensor module comprising of one or more sensors, is electrically connected with the SENTIOF platform through a rigid and strong header interface. In addition, two mounting holes are created in order to provide structural reinforcement of the platform and the sensor module, which may be required for certain applications.

III. Software Design

In order to use the SENTIOF for an application, supporting software must be developed for both the micro-controller and the FPGA. Currently, this is achieved using two different software development environments, the AVR32 Studio and the Xilinx ISE for the micro-controller and FPGA, respectively.

The integrated development environment for the micro-controller that can be obtained from Atmel's website free of charge and it integrates a software framework and a GNU tool chain allowing easy and rapid application development in C/C++. To further enhance the software development process of the micro-controller in relation to the SENTIOF, application programming interfaces (APIs) are developed for all control and data transfer specific operations including power management, radio communication and reading/writing to SD card.

The Xilinx ISE Design Suite integrates all the tools to support complete design development, starting from an RTL design specification to the generation of a programming file for the FPGA. It also includes a wide variety of IP cores that can be integrated into a design, thus resulting in rapid development. In relation to the SENTIOF, we have developed interface APIs for both the SRAM and the FLASH, which can be re-used in other designs. Similar APIs for the radio transceiver and the SD card interface will also be developed in the near future.

IV. Performance and Power Consumption Analysis

The SENTIOF was designed to achieve a high computational performance and low power consumption goals, and these were ensured at each development stage including architectural decisions, component selection, and PCB layout. Performance of both the micro-controller and the FPGA is dependent on an underlying application. Therefore, a measure of clock frequency, on which these two can be operated, is discussed for analysis purposes. However, the precisely measured power consumption for various activities is used for analysis in the this section.

D. Clock frequency

The micro-controller can either be clocked from an internal oscillator producing a clock frequency of about 115 kHz or from an external oscillator producing 16 MHz of clock frequency. The clock from the internal oscillator is often too slow for a computationally intensive application and therefore, may be used in either very low-speed applications or during sleep modes. However, to achieve different performance levels, the micro-controller can be operated at a wide frequency range, with an upper limit of 60 MHz. In such cases, the desired frequency can be synthesized from a 16 MHz external oscillator by using a built-in Phase Locked Loop (PLL) in the micro-controller.

During the SENTIOF design it was observed that the available oscillators with frequencies higher than 19 MHz, as is required in the FPGA, consume a significant amount of power that is undesirable in a low-power platform. Therefore, a global clock generation feature of the micro-controller was instead used to provide the clock for the FPGA. The frequency of this input clock can be further increased to 375 MHz using a PLL in the FPGA.

E. FPGA Configuration

In order to conserve power, it may be desirable to switch off the FPGA for idle time periods in an application. However, upon power-up, it must be reconfigured to resume its job. The (re)configuration for the FPGA integrated in the SENTIOF is accomplished by loading nearly 3.6 Mb of configuration data into the FPGA, from the associated FLASH memory. Depending upon the clock frequency and the bus width options that are selected to configure the FPGA, the actual configuration time can vary from one application to another.

The minimum configuration time of 15.16 ms was recorded by applying a maximum supported speed of 66 MHz and a maximum bus width option of 4 bits, also known as quad SPI.

F. Power Consumption

The power consumption in the SENTIOF can be optimized through dynamic power management, where all major components including the micro-controller, FPGA, SRAM, FLASH, and the radio transceiver can be switched to low-power modes at run time. This allows a reduction in the power consumption of each component to a minimum level, typically from tens of micro-watts to a few milli-watts depending upon the actual component. Therefore, to further minimize the power consumption during the idle state, the SENTIOF is designed to dynamically switch-off/on the FPGA, SRAM, FLASH, and SD card as they consume significant power in their low-power modes. To realize this power on/off mechanism, a very low-power metal-oxide semiconductor (MOS) transistor is used as a switch between the power supply and the power connection of the components. The transistor is then switched on/off through the micro-controller, which performs all control specific operations including power management. It should be noted that radio transceiver that typically consumes 1μW in low-power mode and, it is not enabled to be switched on/off using MOS transceiver, as the MOS transistor consumes almost the same amount of power as that of the radio transceiver in low-power mode and therefore, no significant power can be conserved by the power on/off method.

Depending on the application, the SENTIOF may be in active mode, where it performs data acquisition, processing, and/or result transmission, or it may be in sleep mode for certain time duration before it is operational again. The power consumption in these modes differs significantly and therefore, it is discussed with respect to these two modes in the following.

Sleep mode

In sleep state, with the exception of the micro-controller, other components including the FPGA, SRAM, FLASH, and the SD card are switched-off. The micro-controller however, is switched to a low-power mode known as DeepStop, in which it is not only able to keep track of the sleep duration by using real time counter (RTC), but is also capable of switching all components including itself to the active state.

In sleep mode, the average current drawn by the SENTIOF from a 3.6V supply source was measured to be 95 μA. During this mode, both the 1.8V and 3.3V voltage regulators which remained fully functional to ensure the required voltage levels to the micro-controller were responsible for nearly 70% of the reported current consumption.

Active mode

Unlike the sleep mode, the power consumption of the SENTIOF during its active mode is dependent on an frequencies and the time duration for which different components are active. Nevertheless, to provide a rough idea, the current consumption was measured for a number of application scenarios involving almost all the major components on the SENTIOF, and is summarized in Table II. Each reported value represents the total amount of current that was drawn by the SETNIOF for a corresponding scenario, from a 3.6V power source.

For application scenarios 1, 2, and 3 given in Table II, the micro-controller was in the active state performing a simple addition operation repeatedly. Apart from the 3.3V and 1.8V voltage regulators that are required to provide power to the mi-

TABLE II. THE AVERAGE CURRENT CONSUMPTION OF THE SENTIOF FOR DIFFERENT APPLICATION SCENARIOS

S. No.	Actions	Average Current (mA)
1.	The micro-controller is clocked at 16 MHz and is in active mode, where it performs an addition operation repeatedly.	5.54
2.	Same as of 1, except the clock frequency is 20 MHz.	7.49
3.	Same as of 1, except the clock frequency is 60 MHz.	21.34
4.	The micro-controller is clocked at 16 MHz and is in Frozen mode, in which it generates 20 MHz of clock frequency for the FPGA.	4.28
5.	Same as of 4 + both the FPGA and the Flash are ON, and the FPGA loads bit-stream from the FLASH at 66 MHz using quad SPI interface.	30.3
6.	Same as of 4 + FPGA is active and is running a design in which, a 100 MHz of clock is synthesized through internal PLL, and then is used to update a 27-bit counter.	22.31
7.	Same as of 6, except that the FPGA is in standby mode.	8.30
8.	Same as of 6 + the FPGA reads 16-bit data word from the SRAM repeatedly at a rate of 16.6 MHz.	34.58
9.	Same as of 6 + the FPGA writes 16-bit data word to the SRAM repeatedly at a rate of 16.6 MHz.	44.62
10.	Same as of 6 + the FPGA erases the FLASH memory.	48.17
11.	Same as of 6 + the FPGA reads data from the FLASH memory at a rate of 50 MHz.	29.90
12.	Same as of 6 + the FPGA writes data to the FLASH memory.	38.89
13.	Same as of 2 + the micro-controller reads data from the SD card at a rate of 20 MHz.	20.64
14.	Same as of 2 + the micro-controller writes data to the SD card at a rate of 20 MHz.	24.37
15.	Same as of 1 + the radio transceiver operates in receive mode and received packets are transferred to the micro-controller.	31.34
16.	Same as of 1 + the data packets from the micro-controller are transmitted by the radio transceiver at rate of 250 kpbs using 5 dBm power.	39.15

cro-controller, all other modules were in the off state. The micro-controller was clocked through a 16 MHz external oscillator, and then synthesized to 20 MHz and 60 MHz through an internal PLL.

The average current drawn by the SENTIOF while configuring the FPGA from the associated FLASH is given in Scenario 5. Scenarios 8 and 9 list the current consumption when the FPGA performs read and write operations on the SRAM. Other important scenarios include 15 and 16, in which the radio transceiver is operated in receive and transmit modes, respectively.

V. Conclusion

In this paper, we presented a high-performance and low-power wireless hardware platform, SENTIOF that is capable of performing high-throughput in-sensor processing, as typically required for high-sample rate monitoring applications.

The SENTIOF integrates a micro-controller, an FPGA, an SRAM, a FLASH, and a radio transceiver on a single PCB in order to realize a high-performance compact wireless platform. This application independent platform allows for the integration of any kind of sensors through an application specific and customized sensor layer. In addition, the dynamic power management and reconfigurable architecture can be exploited to optimize performance and power consumption according to different applications.

The flexibility provided through dynamically configurable interfaces, customizable communication between the micro-controller and the FPGA, and dynamic power management can also be used to explore efficient architectures for different monitoring applications.

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