

Analyzing Control Structures of SSSCs for Fast Compensation in the Case of Unbalanced Voltage Sag in Power System

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Abstract—Fast compensation of voltage sag on the three-phase electric power caused by different faults is a problem studied to ensure that loads work normally. This paper introduces two vector control structures for Series synchronous static compensators (SSSC): the PI controller on the dq reference frame and the Sequence-decoupled resonant (SDR) controller on the $\alpha\beta$ reference frame. An analysis was performed to compare the two control structures to evaluate their qualities and advantages. Based on that conclusion, we propose a solution to apply suitably to controllers of SSSC devices. The control structures are simulated in Matlab/Simulink. The simulation results verified our analyses and evaluations. From there, this paper presents a recommended control structure for SSSC.

Index Terms—Dynamic voltage restorer, Voltage sag, Power quality.

I. INTRODUCTION

Voltage sag and the harmonics on the power grid are defined in IEEE Std. 1159-1995. These are serious problems, which are related to power quality. Furthermore, its frequency is the highest among all types of grid faults with 31% for voltage sag and 18% for harmonics [1]. Figure 1 shows a voltage sag in the power system and Fig. 2 shows its effects on electrical equipment and systems.

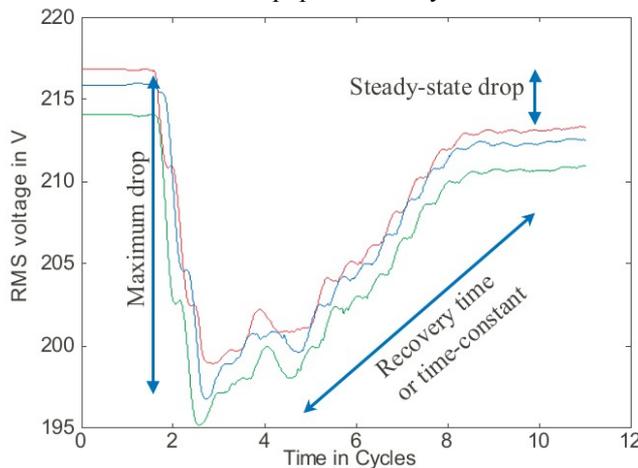


Fig. 1. Three-phase voltage sag [2].

Voltage sag is a type of disturbance that occurs unpredictably and depends on various faults occurring in the power system, for example, especially short circuit faults. Voltage sag occurs during small time and has voltage amplitude and phase angle variations that change rapidly and continuously during the faults.

The effect of voltage sag seriously affects the loads and is one of the causes of economic losses. The results of a power quality survey about the effects of voltage sag and harmonics of electricity consumers in 1,400 locations in 8 countries [1] are shown in Fig. 2.

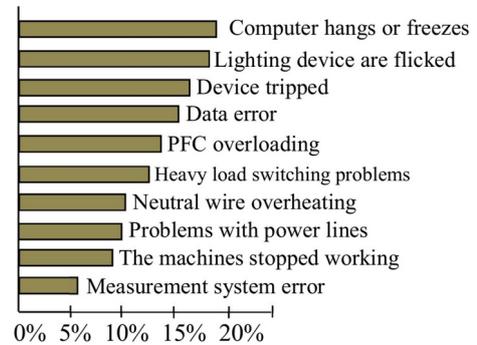


Fig. 2. Effects of voltage sag to electrical equipment and systems [2]

To solve this problem, there are many solutions to have been presented such as Generator – engines; Transformer-based regulator devices; Static switches; UPS systems; Series synchronous static compensators (SSSCs); D-Stacom. However, SSSCs are considered a highly efficient solution and the most suitable choice for consumers [2].

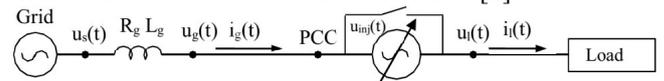


Fig. 3. Schematic of the operation principle of SSSC [3]

Basically, the SSSC is designed to be connected in series between the source and the load (Fig. 3). The SSSC is considered a voltage source whose magnitude, phase angle and frequency can be adjusted through an inverter.

The principle of regulating and stabilizing the load voltage of the SSSCs (u_L) is shown in Fig. 4. Where, i_l is the load current vector; φ is the phase difference angle between the load voltage and the load current; ψ is the phase jump angle of the load voltage, it is referenced to the grid voltage during voltage sag.

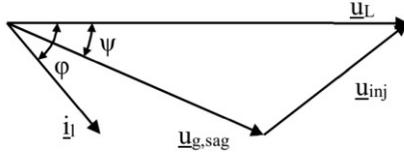


Fig. 4. Vector diagram of the sag compensation principle of SSSC [3]

When a voltage sag occurs, the SSSC will generate an injectable voltage (u_{inj}) whose magnitude and phase angle are determined by the controller. The load voltage becomes:

$$\vec{u}_L = \vec{u}_{g,sag} + \vec{u}_{inj} \quad (1)$$

The parameter of the voltage vector will depend on the rate of change of the grid voltage (u_{gsag}) and will be determined by the controller of the SSSCs.

In fact, when a voltage sag occurs, the rate of balanced voltage sag is approximately 5% and one of unbalanced voltage sag is approximately 95% [1,2]. A very important issue in control is that the balanced voltage sag just had to inject the positive sequence components, while the unbalanced voltage sag must inject positive sequence components, negative sequence components and zero sequence components. Therefore, when designing the controller, this issue should be taken into account. The solution for this problem is that we need to implement separately the sequence components to control. Figure 5 shows a diagram vector of positive sequence components and negative sequence components of the source voltage.

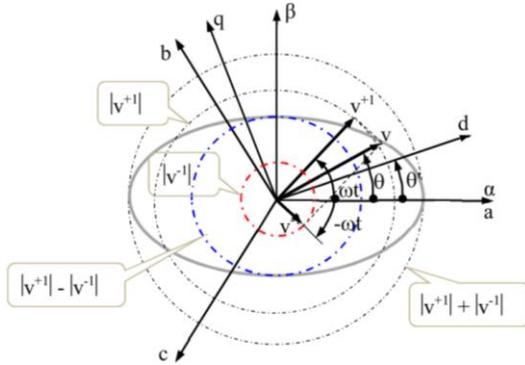


Fig. 5. Vector diagram of source voltage in the unbalanced voltage sag [4]

Where, the vector v is the voltage of the power system, which is separated by the sum of the positive sequence component v^{+1} and the negative sequence v^{-1} .

The vector v contains information for both the positive and negative sequence components. Therefore, the control of the voltage vector v will be replaced by the control of two vectors: the positive sequence component v^{+1} and the negative sequence component v^{-1} .

A control structure for an SSSC in case of unbalanced voltage sag is built as shown in Fig. 6.

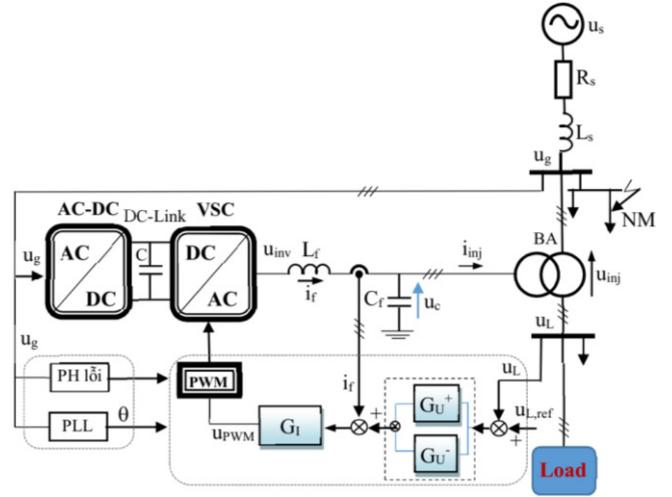


Fig. 6. SSSC control structure with current feedback from the inverter.

Where, N - three-phase electric power; R_s, L_s are source resistance, source inductance, respectively; u_g is the voltage of power grid; u_L is load voltage, BA is a series transformer; L_f, C_f is filter inductance, filter capacitor, respectively; AC/DC is rectifier converter; VSC-DC/AC is inverter; DC-link is DC bus; PH is voltage sag detector; PLL is phase-locked loop; G_{U+}, G_{U-} are positive and negative sequence components voltage controller; G_I is current controller; PWM is pulse width modulator; i_f is current feedback signal; u_L is load voltage feedback signal; $u_{L,ref}$ reference load voltage.

The SSSC control structure shown in Fig. 6 can be designed based on abc reference frame or dq reference frame or $\alpha\beta$ reference frame [5].

There are many controllers that have applied this structure to SSSC [5,6,7,8]. Two prominent controllers of them are PI controller for reference frame dq and Sequence Decoupled Resonant (SDR) for $\alpha\beta$ reference frame.

II. THREE-PHASE SSSC CONTROL STRUCTURE IN CASE OF UNBALANCED MAINS VOLTAGE SAG

A. The vector control structure cascades on the dq reference frame to the PI controller

The control structure is built based on the vector control principle in Fig. 7.

In this structure, the current control loop of the LC filter directly affects the compensating power of the SSSC. The control loop of injection voltage controls the load voltage following the reference load voltage ($u_{L,ref}$). The current controller G_I and voltage controller G_U are PI controllers. The transformation abc to $\alpha\beta$, $\alpha\beta$ to dq and a phase-locked loop (PLL) are important components of the control structure.

Projecting the vectors in equation (1) onto the dq reference frame, the reference value of the injection voltage is determined as follows:

$$u_{inj}^{dq} = u_C^{dq} = u_L^{dq} - u_s^{dq} \quad (2)$$

The actual insertion voltage (u_{inj}) is also the voltage across the capacitor of the LC filter.

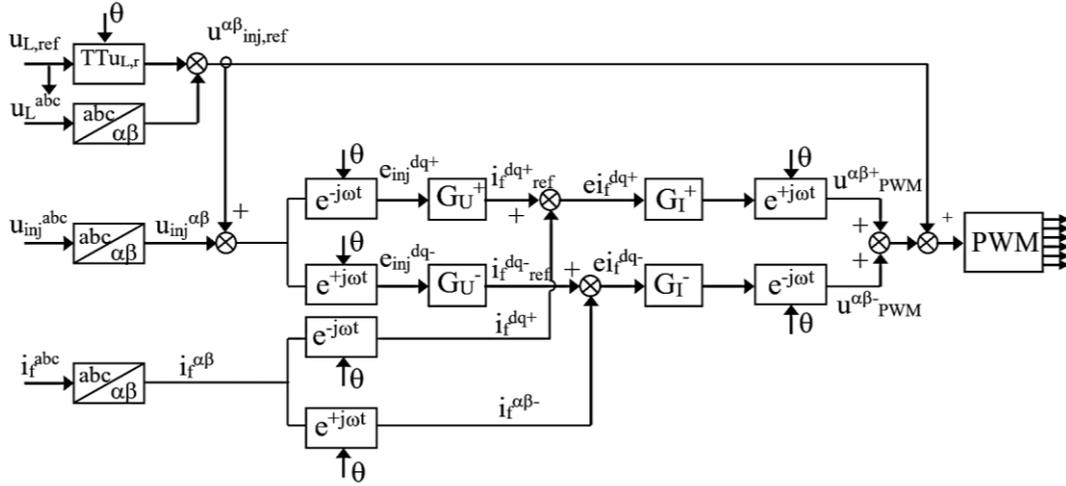


Fig. 7. SSSC control structure on rotation dq reference frame.

- **Current control loop**

The positive and negative sequence current components are separated for control.

Positive sequence current control loop:

$$u_{inv}^{dq+}(k) = u_{inj}^{dq+}(k) + R_f i_f^{dq+}(k) \mp j\omega L_f i_f^{dq-}(k) + G_I^+ \frac{L_f}{T_s} (i_f^{dq+}(k+1) - i_{inj}^{dq+}(k)) \quad (3)$$

Negative sequence current control loop:

$$u_{inv}^{dq-}(k) = u_{inj}^{dq-}(k) + R_f i_f^{dq-}(k) \pm j\omega L_f i_f^{dq+}(k) + G_I^- \frac{L_f}{T_s} (i_f^{dq-}(k+1) - i_{inj}^{dq-}(k)) \quad (4)$$

Where: G is the transfer function of the discrete controller Integral – Proportional.

- **Voltage control loop**

The positive and negative sequence voltage components are separated for control.

Positive sequence voltage control loop:

$$i_f^{dq+}(k+1) = i_{inj}^{dq+}(k) + G_U^+ \frac{C_f}{T_s} (u_{inj}^{dq+}(k) - u_{inj}^{dq+}(k)) - u_{inj}^{dq+}(k) \pm j\omega C_f u_{inj}^{dq-}(k) \quad (5)$$

Negative sequence voltage control loop:

$$i_f^{dq-}(k+1) = i_{inj}^{dq-}(k) + G_U^- \frac{C_f}{T_s} (u_{inj}^{dq-}(k) - u_{inj}^{dq-}(k)) - u_{inj}^{dq-}(k) \mp j\omega C_f u_{inj}^{dq+}(k) \quad (6)$$

B. SSSC control structure on $\alpha\beta$ reference frame with SDR controller

The control structure is simpler because it uses a quadratic resonant regulator that can handle the positive and negative sequence components separately as shown in Fig. 8.

- **Current control loop**

The equation describing the current loop by using a resonant controller is as follows:

$$u_{inv,ref}^{\alpha\beta}(k+1) = u_{inj}^{\alpha\beta}(k) + (G_{I-SDR}^+ \frac{L_f}{T_s} (i_f^{\alpha\beta}(k) - i_f^{\alpha\beta}(k)) + G_{I-SDR}^- \frac{L_f}{T_s} (i_f^{\alpha\beta}(k) - i_f^{\alpha\beta}(k))) \quad (7)$$

- **Voltage control loop**

The equation describing the voltage loop by using a resonant controller is as follows:

$$i_f^{\alpha\beta*}(k+1) = i_{inj}^{\alpha\beta}(k) + (G_{U-SDR}^+ \frac{C_f}{T_s} (u_{inj,ref}^{\alpha\beta}(k) - u_{inj}^{\alpha\beta}(k)) + G_{U-SDR}^- \frac{C_f}{T_s} (u_{inj,ref}^{\alpha\beta}(k) - u_{inj}^{\alpha\beta}(k))) \quad (8)$$

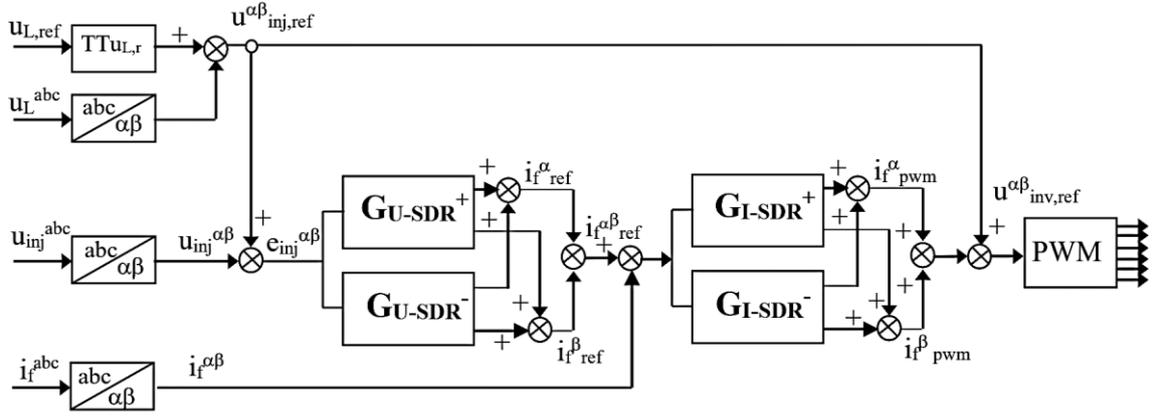
Where,

G_{U-SDR}^+ , G_{I-SDR}^+ - are the voltage and current resonance controller for the positive sequence component, respectively.

G_{U-SDR}^- , G_{I-SDR}^- - are the voltage and current resonance control for the negative sequence component, respectively.

In the introduced control structure, the SDR regulator is equivalent to conventional resonant controllers but it can be built with the MIMO control structure, which is easier to implement. The SDR controller has been described detailed and designed in [3, 8].

The SDR controller with multiple inputs and multiple outputs is described as follows:

Fig. 8. SSSC control structure on $\alpha\beta$ reference frame.

$$y_{\alpha 1}^+(s) = \frac{1}{s} [K_I \cdot e_{\alpha}(s) - \omega_1 \cdot y_{\beta 1}^+(s)] \quad (9)$$

$$y_{\beta 1}^+(s) = \frac{1}{s} [K_I \cdot e_{\beta}(s) + \omega_1 \cdot y_{\alpha 1}^+(s)]$$

$$y_{\alpha 1}^-(s) = \frac{1}{s} [K_I \cdot e_{\alpha}(s) + \omega_1 \cdot y_{\beta 1}^-(s)] \quad (10)$$

$$y_{\beta 1}^-(s) = \frac{1}{s} [K_I \cdot e_{\beta}(s) - \omega_1 \cdot y_{\alpha 1}^-(s)]$$

According to this method, the equations described in equations (9) and (10) can be easily performed on the $\alpha\beta$ reference frame in the time domain by digital methods.

Figure 9 shows the implementation structure diagram of the controller to control positive or negative sequence voltage components or both.

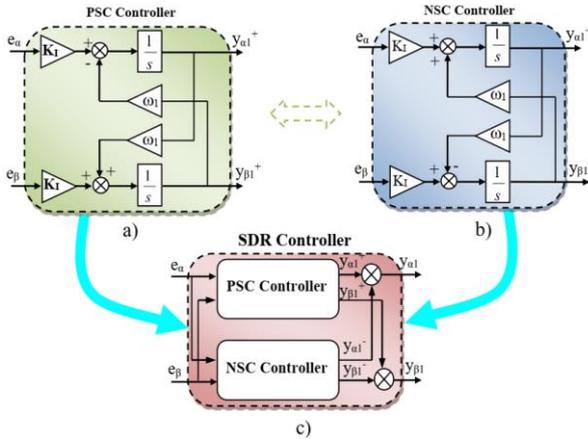


Fig. 9. Structure diagram of the SDR controller on $\alpha\beta$ reference frame .
a) Positive sequence component controller b) Negative sequence component controller c) both sequence components [4,7].

III. SIMULATION RESULTS

A. Case 1: Compensation for unbalanced voltage sag

An unbalanced voltage sag occurs on the grid between $t = 0.12s$ and $t = 0.25s$. The amplitude of voltage sag in phases is not equal: phase C 40%, phase B 10%.

Source voltage u_s

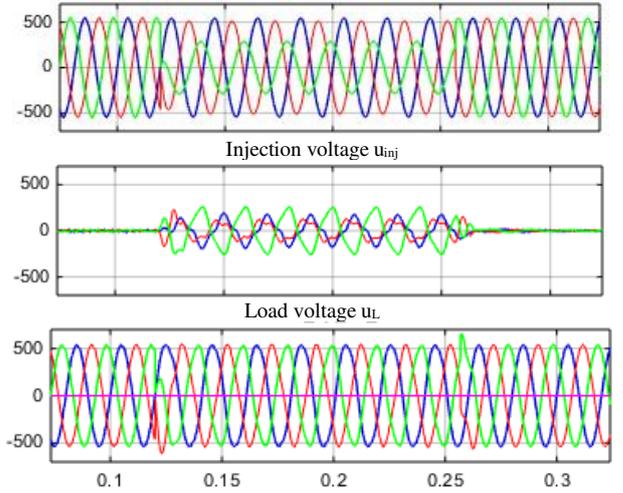


Fig. 10. Simulation results of SSSC using control structure on dq reference frame in case of unbalanced voltage sag.

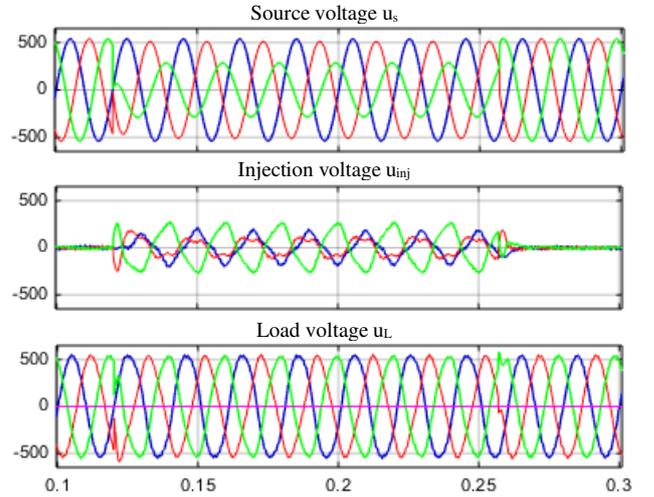


Fig. 11. Simulation results of SSSC using control structure on dq reference frame in case of unbalanced voltage sag.

Figure 11 shows the difference between the reference load voltage and the actual load voltage of the two control structures during the time period from $t = 0.12s$ to $t = 0.25s$. The results show that the error of the two structures is approximately zero. The results also show that the actual load voltage follows exactly the reference value.

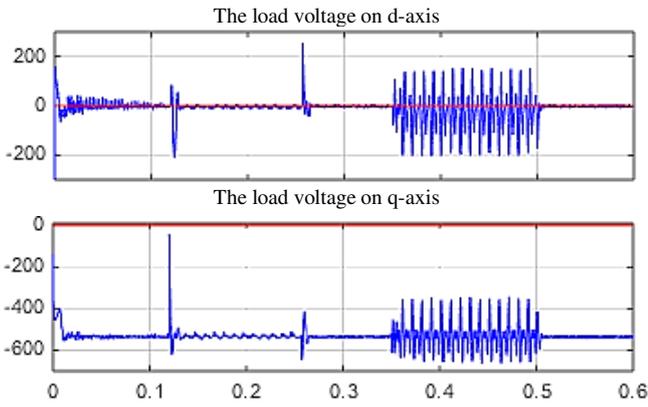


Fig. 12. Simulation results of the load voltage of the control structure on the dq reference frame .

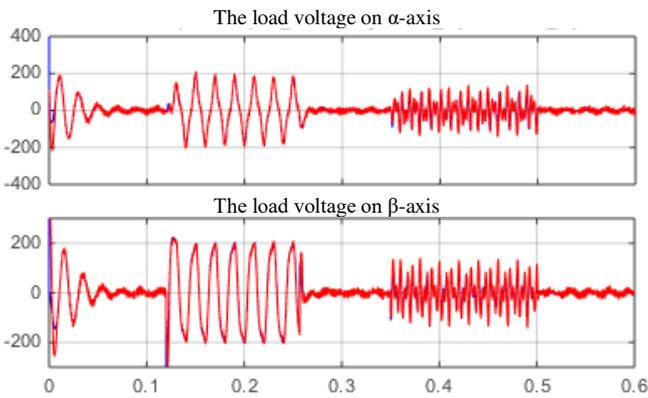


Fig. 13. Simulation results of the load voltage of the control structure on the $\alpha\beta$ reference frame .

Fig.12 shows the result of harmonic spectrum and total harmonics (THD) of the load voltage of both control structures during the period from 0.12s to 0.25s.

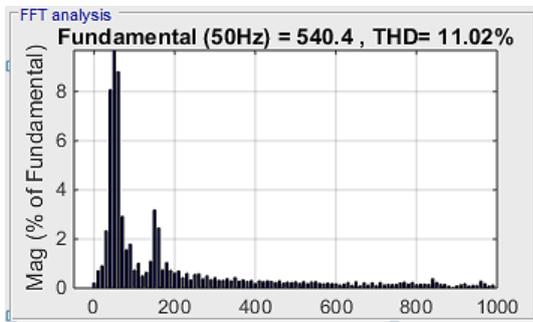


Fig. 14. Harmonic analysis results of SSSC using control structure on dq reference frame .

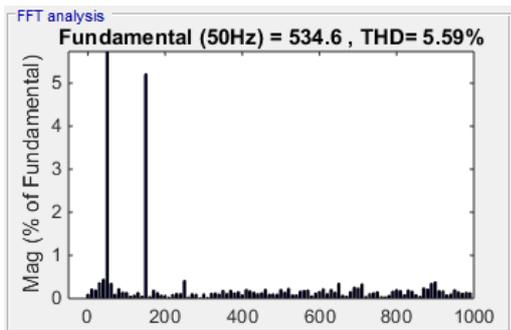


Fig. 15. Harmonic analysis results of SSSC using control structure on $\alpha\beta$ reference frame .

While harmonic spectrum of the structure using the PI controller includes: 3th-0.5%, 5th-3%, 7th-6%, THD = 11.02%, the ones of structure using the SDR controller includes harmonic: 3th-0.5%; 5th-3%; 7th-6%. THD = 5.59%.

B. Case 2: Compensation for unbalanced voltage sag containing harmonic components in the fault.

A voltage sag occurs during from 0.12s to 0.25s. Addition, during 0.17s to 0.3s, harmonic components: 3th = -10%, 5th = -10% are added.

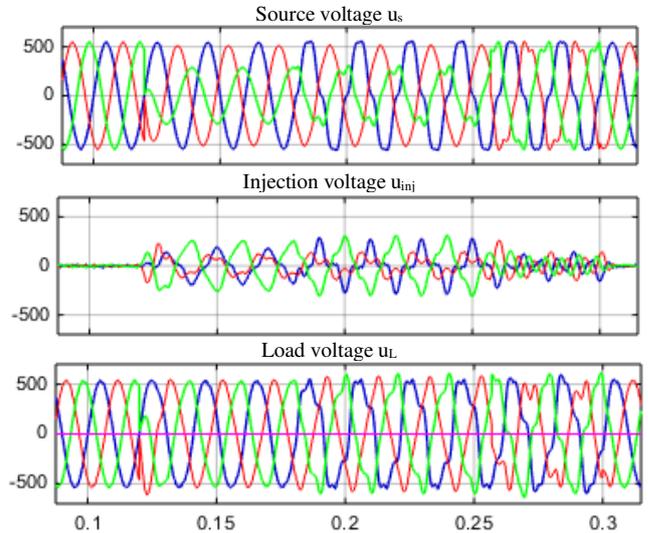


Fig. 16. Simulation results of unbalanced voltage sag compensation of SSSC using control structure on dq reference frame .

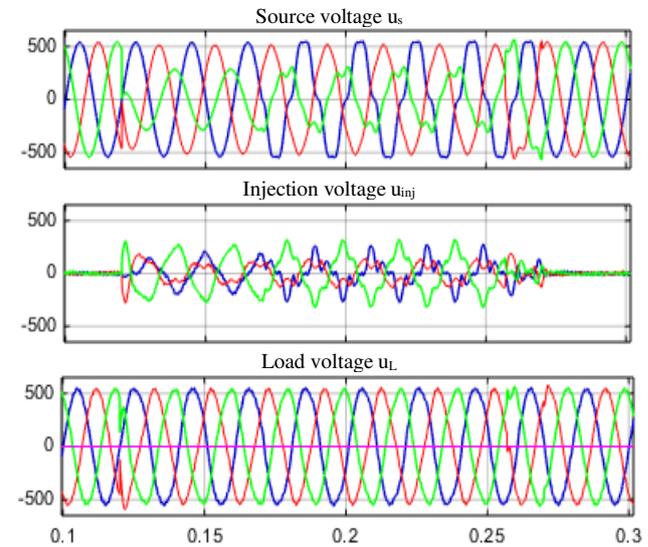


Fig. 17. Simulation results of unbalanced voltage sag compensation of SSSC using control structure on alpha-beta reference frame .

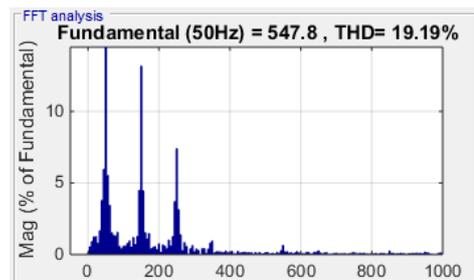


Fig. 18. Harmonic analysis results of SSSC using control structure on dq reference frame .

Figure 18 shows the results of the analysis of the harmonic spectrum and the total harmonics of the load voltage while the voltage sag was occurring. The results show that the load voltage in the control structure on the dq reference frame includes harmonic components: 3th-10%, 5th-10%, 7th-6% and the total harmonics increased from 14.56% (pre-sag) to 19.19% (in-sag).

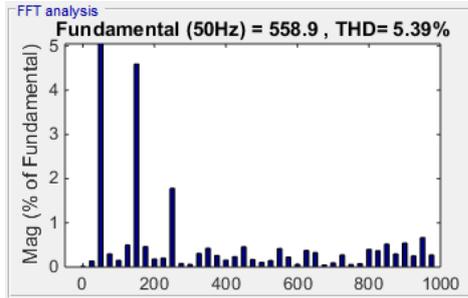


Fig. 19. Harmonic analysis results of SSSC using control structure on $\alpha\beta$ reference frame .

Meanwhile, the load voltage in the control structure on the $\alpha\beta$ reference frame using the SDR controller include harmonic components: 3th-10%, 5th-10% and the total harmonics are reduced from 14.56% (pre-sag) to 5.39% (in-sag).

Remark 1: The vector control structure on the reference frame dq , which uses PI controllers, is capable of controlling the positive and negative sequence components independently. The control signals on this structure are DC signals. Therefore, this system is capable of making tolerance to 0. However, this control structure requires 8 PI controllers for 4 control channels and has to use 6 $\alpha\beta/dq$ transformations and 4 change $abc/\alpha\beta$ transformations. The results show that this control structure is capable of fast compensatory response, which is approximately from 0.005s to 0.01s (Fig. 10, Fig. 16 and 17). The load voltage is balanced and follows the reference voltage. Total harmonics are 11.02% (Fig. 14). However, the ability compensation in case of including harmonic components of this structure is not high quality, and the load voltage is not pure sine (Fig. 10, Fig. 16 and 17).

Remark 2: The vector control structure on the $\alpha\beta$ reference frame with the SDR controller is capable of controlling the sequence components on the $\alpha\beta$ reference frame independently. The reason of this problem is that its controller is built as a MIMO structure. Adjustment of controller parameters can be done independently for each sequence component. Therefore, the SDR controller has the ability to

calibrate more precisely. The results show that the load voltage follows the reference voltage, the load voltages are balanced and the total harmonics of the load voltage are small, 5.59%. In addition, it is capable of compensating both voltage drop and harmonics effectively. The total harmonics of the load voltage are reduced from 14.56% to 5.39% (Fig. 12). The control structure on the $\alpha\beta$ reference frame with the SDR controller is simple and easy to implement.

IV. CONCLUSION

This paper analyzes and evaluates two control structures of SSSCs for fast compensation of balanced and unbalanced voltage sag. Vector control structure on dq reference frame with PI controller and vector control structure on $\alpha\beta$ reference frame with SDR controller was applied. Following the result of analysis, simulation and evaluation, the vector control structure on the $\alpha\beta$ reference frame with SDR controller which has many advantages is recommended to use for SSSCs.

REFERENCES

- [1] Bhattacharyya, S., Myrzik, J. M. A., & Kling, W. L. (2007, September). Consequences of poor power quality-an overview. In 2007 42nd International Universities Power Engineering Conference (pp. 651-656). IEEE.
- [2] Strzelecki, R. M. (Ed.). (2008). Power electronics in smart electrical energy networks. Springer Science & Business Media.
- [3] Duy, T. T., Tien, D. V., Gono, R., & Leonowicz, Z. (2016, June). Mitigating voltage sags due to short circuits using dynamic voltage restorer. In 2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC) (pp. 1-6). IEEE.
- [4] Ye, J., Gooi, H. B., Wang, B., Li, Y., & Liu, Y. (2019). Elliptical restoration based single-phase dynamic voltage restorer for source power factor correction. Electric Power Systems Research, 166, 199-209.
- [5] Wang, F., Benhabib, M. C., Duarte, J. L., & Hendrix, M. A. (2009, February). Sequence-decoupled resonant controller for three-phase grid-connected inverters. In 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition (pp. 121-127). IEEE.
- [6] Vo Tien, D., Gono, R., Leonowicz, Z., Tran Duy, T., & Martirano, L. (2018). Advanced control of the dynamic voltage restorer for mitigating voltage sags in power systems. Advances in Electrical and Electronic Engineering, 16(1), 36-45.
- [7] Duy, T. T., Trung, T. B., & Tien, D. V. (2021, August). Voltage Sag Reduction using a Dynamic Voltage Restorer under Different Types of Faults in The Power System. In 2021 International Conference on System Science and Engineering (ICSSE) (pp. 246-251). IEEE.
- [8] Lee, G. M., Lee, D. C., & Seok, J. K. (2004). Control of series active power filters compensating for source voltage unbalance and current harmonics. IEEE Transactions on industrial electronics, 51(1), 132-139.